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Intel -KabyLake-S plamform

CPU:

LGA1151
CPU POWER PAK *3 Phase
GT POWER PAK *2 Phase

Onboard Chip:

HD Audio Codec: ALC887
SIO: NCT5565D
Flash ROM: SPI 64 MB
DP to VGA: ITE6516
CLR_COMS:SLG4B41231

Main Memory:

DDR4 * 2 (Dual Channel)

ACPI:

5VDAUL:uP7501
5VDIMM:uP7501
3VSB:GS7133
3VDSW:GS7116

Expansion Slots:

PCI Express (X16) Slot * 1
PCI Express (X1) Slot * 2
M.2 Slot * 1

ATX:226*185
Ver: 10

System Chipset:

Kaby Lake B250

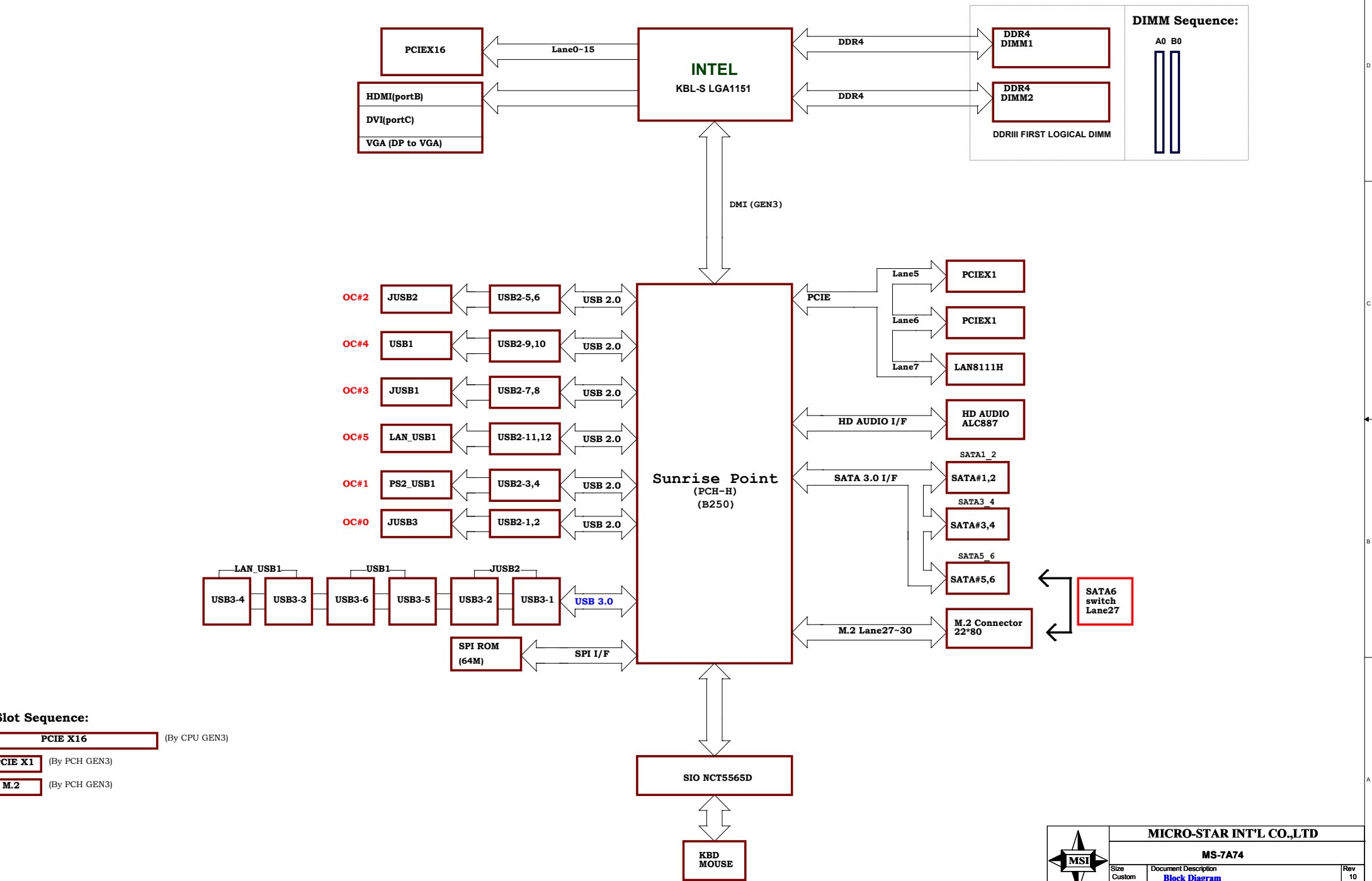
PWM:

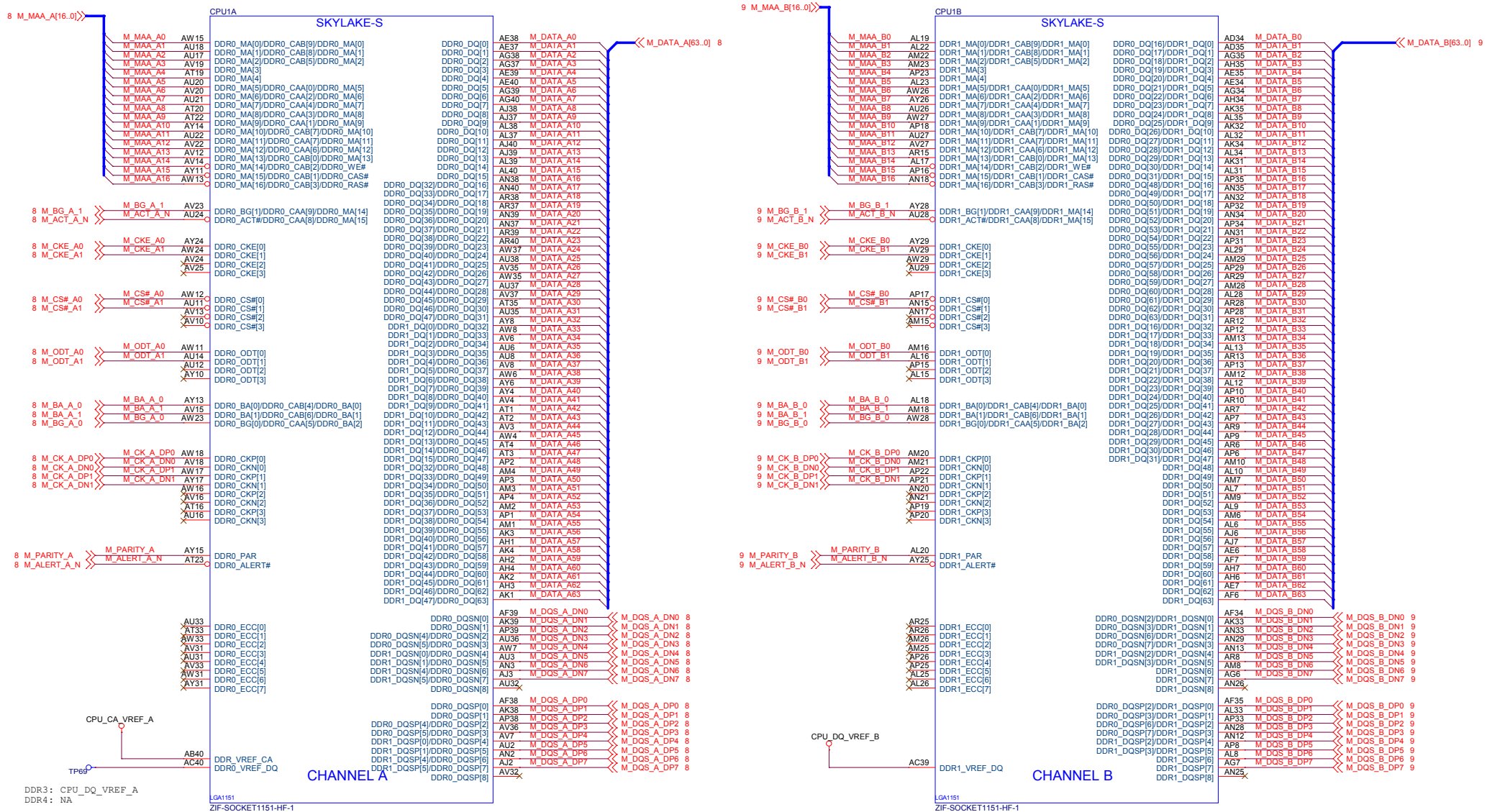
VCORE - RT3606
DDR - RT8231
DDR VPP25- MP2143
PCH(1.0V) - RT8125E
VCCSA - RT8125E
VCCIO - MP5077(Load Switch)

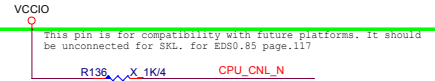
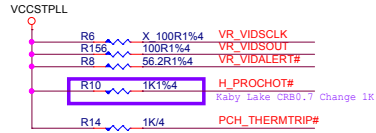


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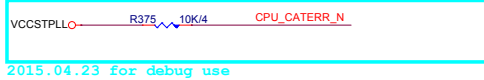
MS-7A74 Block Diagram







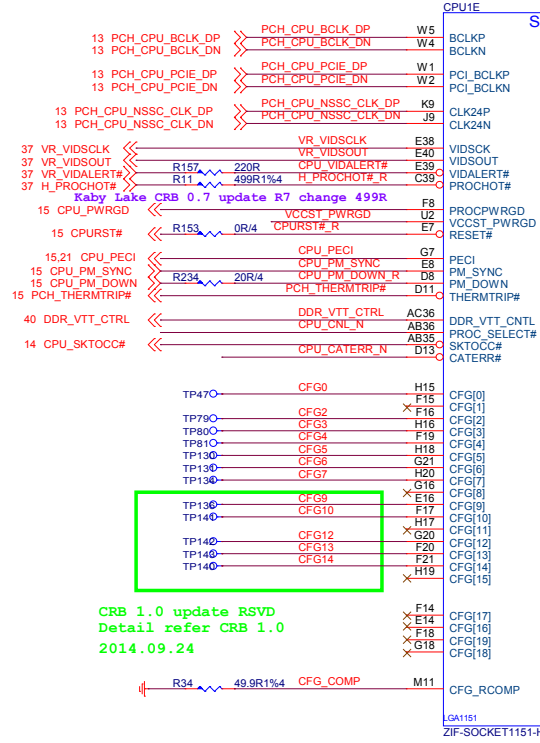
2014.08.14



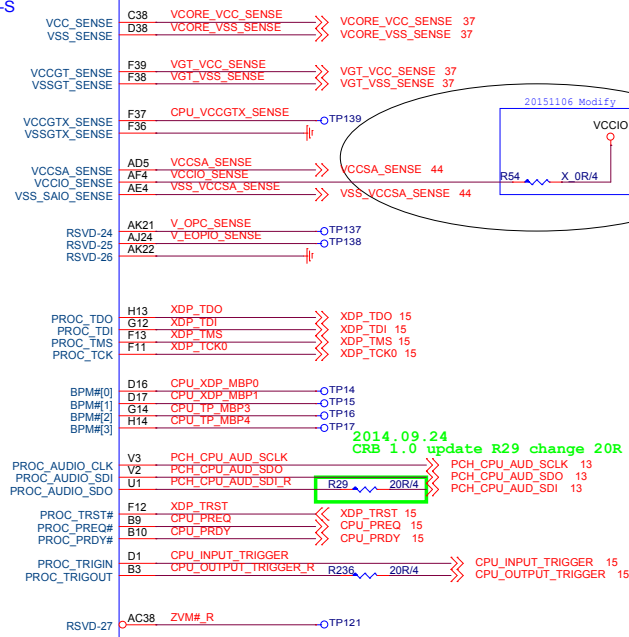
2015.04.23 for debug use

CFG Strap

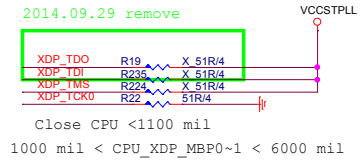
CFG Table			
	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	PCU PLL Lock
1		RSVD	RSVD
2	WORM	REVERSE	PEG LANE REVERSAL
3		RSVD	RSVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PEGOCFGSEL(0)
6	DISABLE	ENABLE	PEGOCFGSEL(1)
7	RESET#	BIOS REQ	PEG DEFER TRAINING
8		RSVD	RSVD
9		RSVD	RSVD
10		RSVD	RSVD
11		RSVD	RSVD
12		RSVD	RSVD
13		RSVD	RSVD
14		RSVD	RSVD
15		RSVD	RSVD



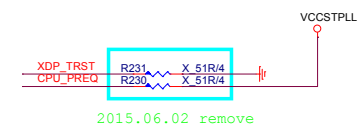
CRB 1.0 update RSVD
Detail refer CRB 1.0
2014.09.24



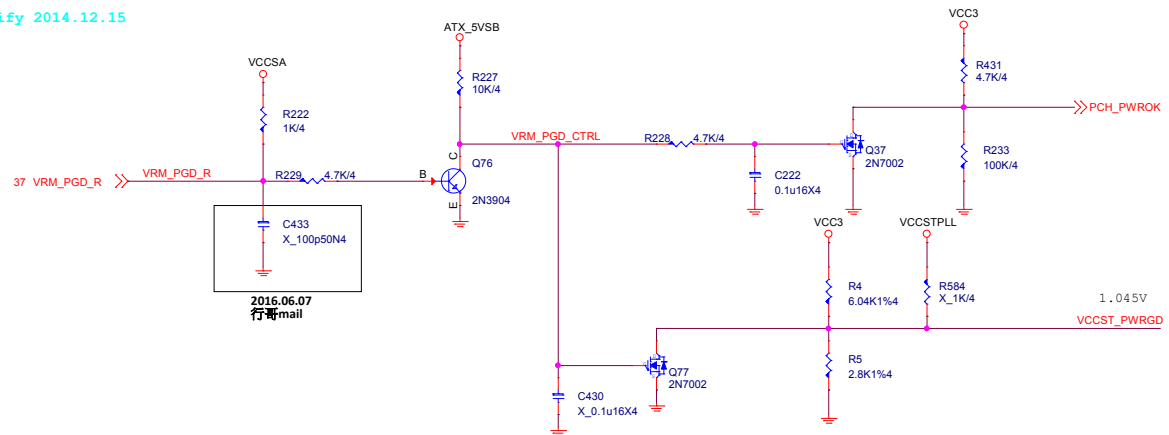
2014.09.24
CRB 1.0 update R29 change 20R



Close CPU <1100 mil
1000 mil < CPU_XDP_MBP0~1 < 6000 mil

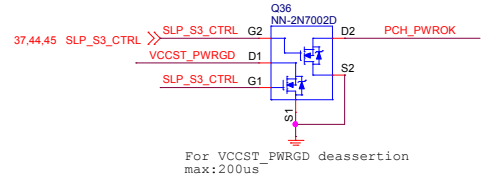


modify 2014.12.15

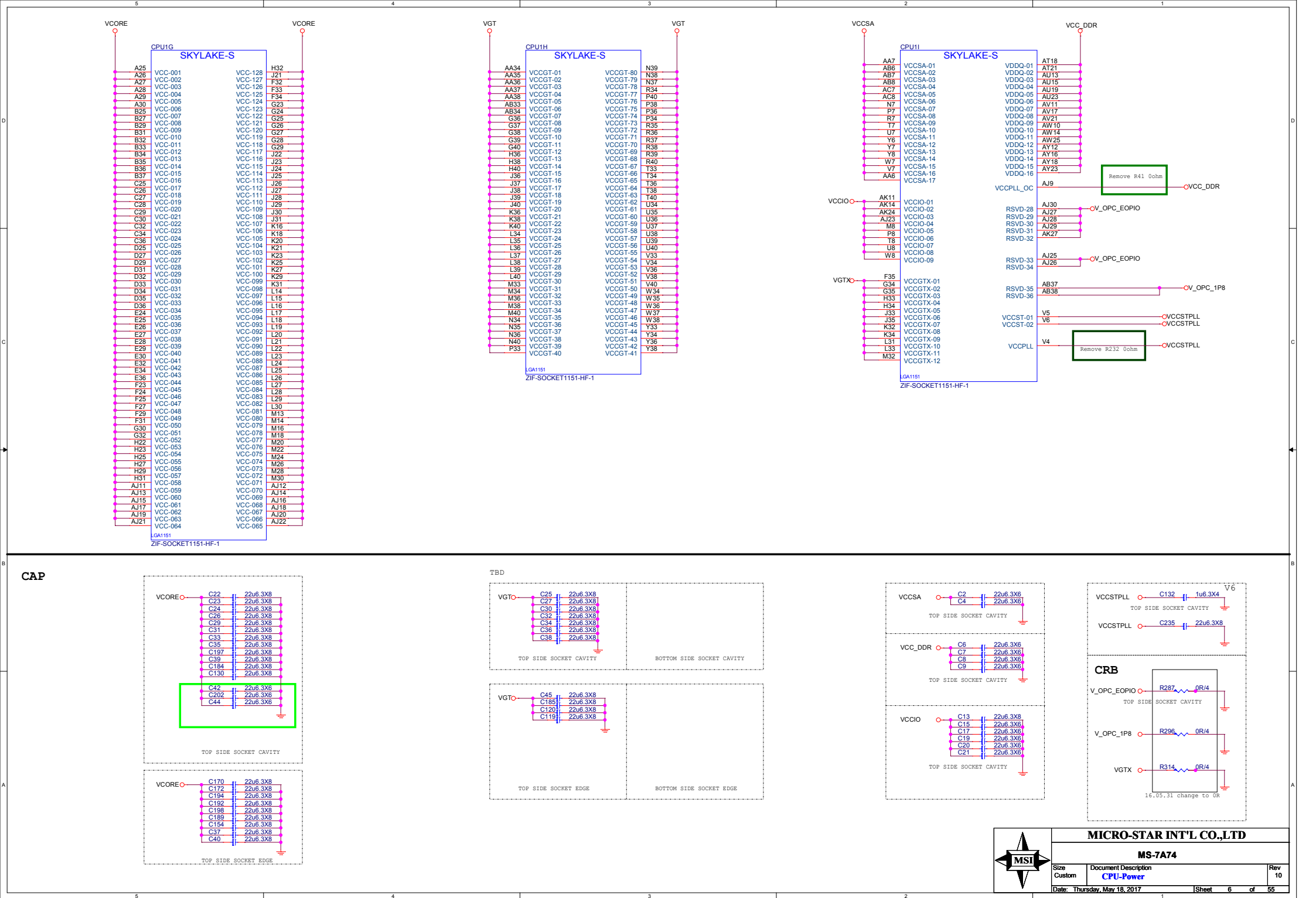


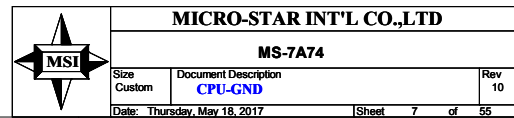
modify 2014.09.19

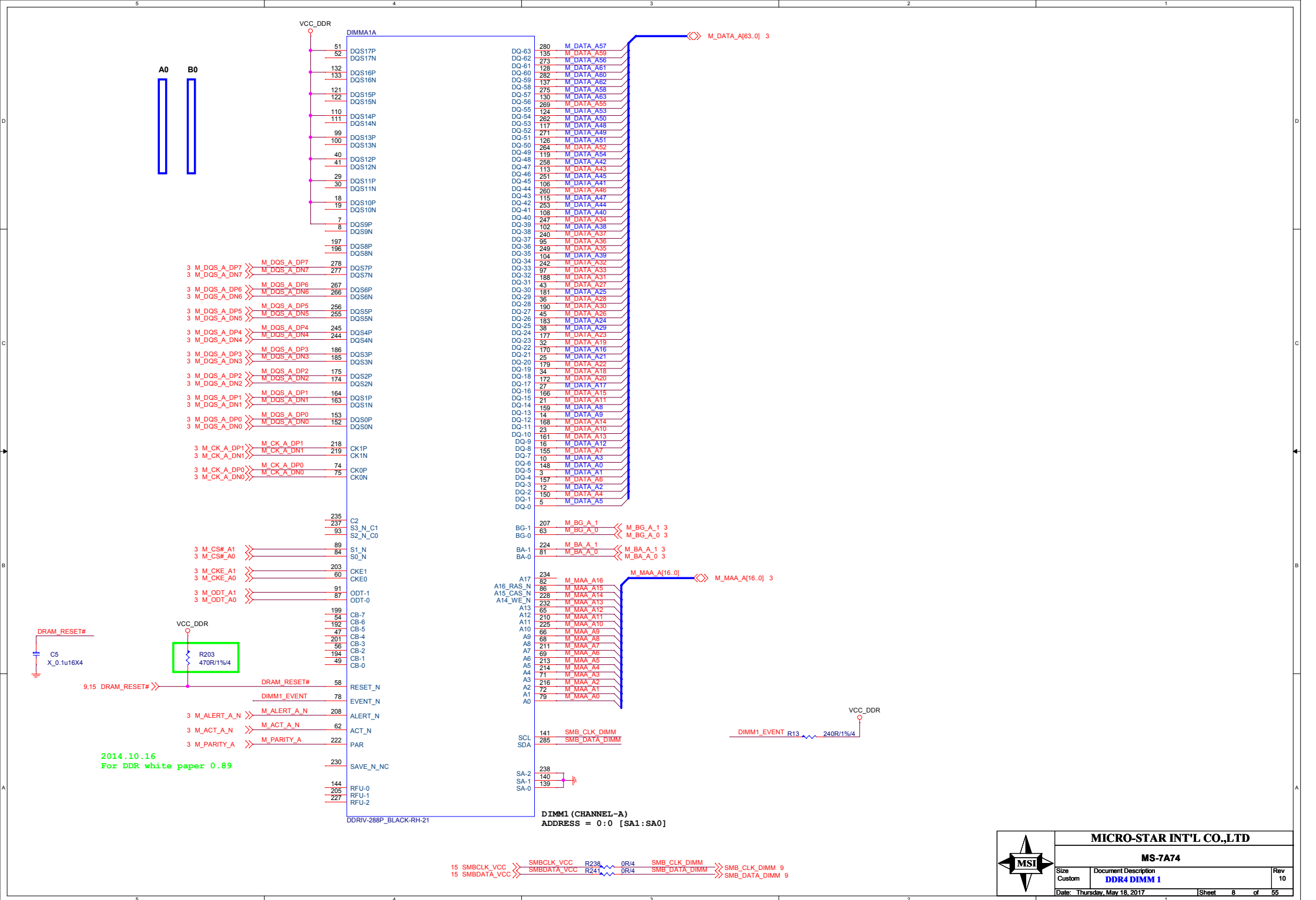
POWER DOWN

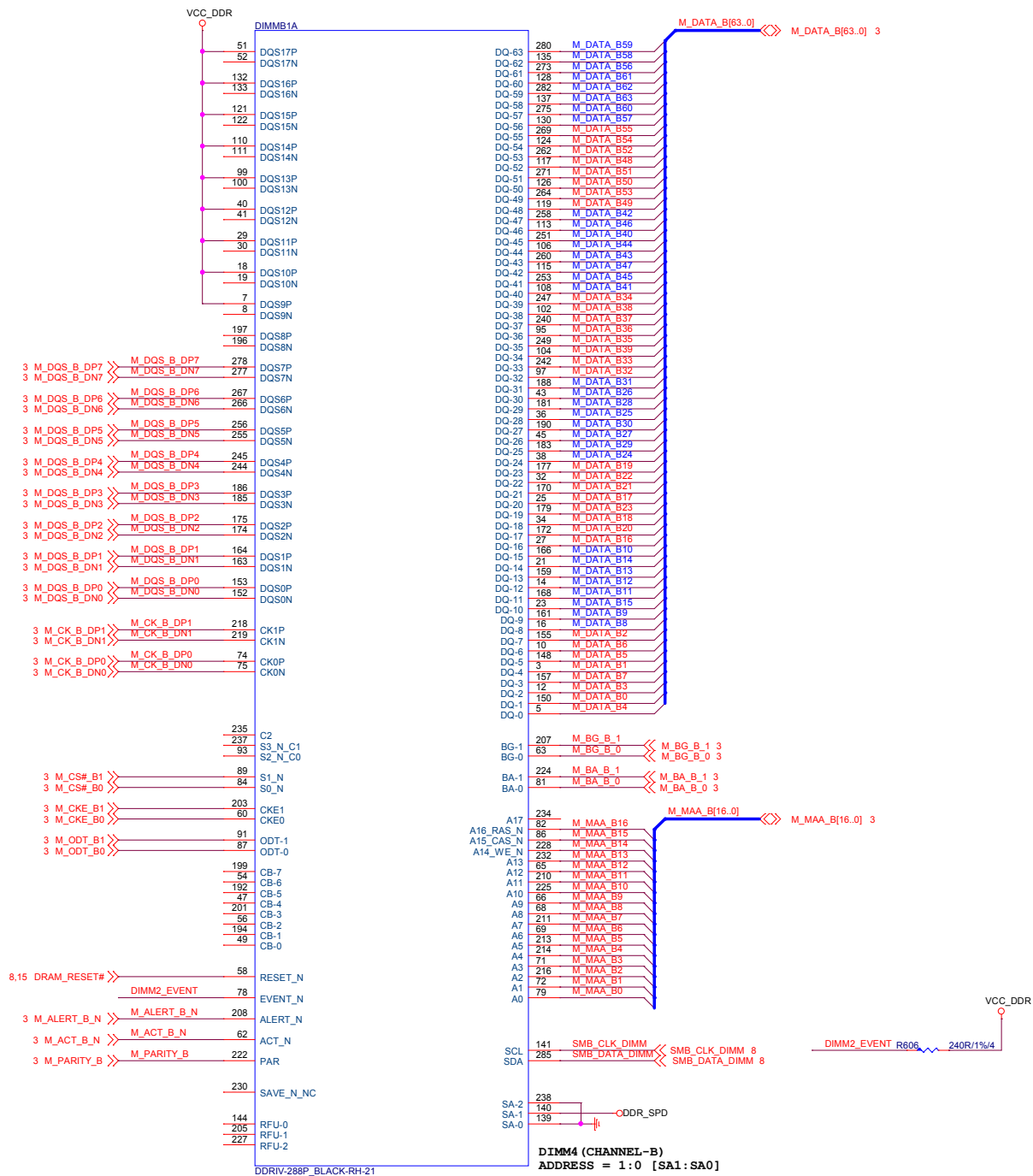


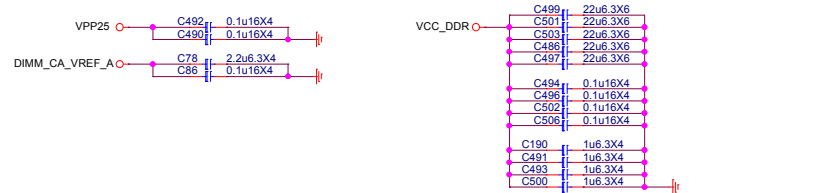
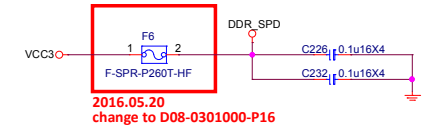
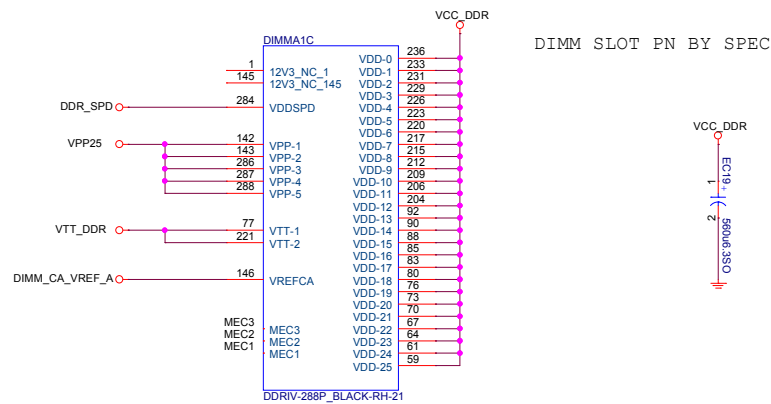
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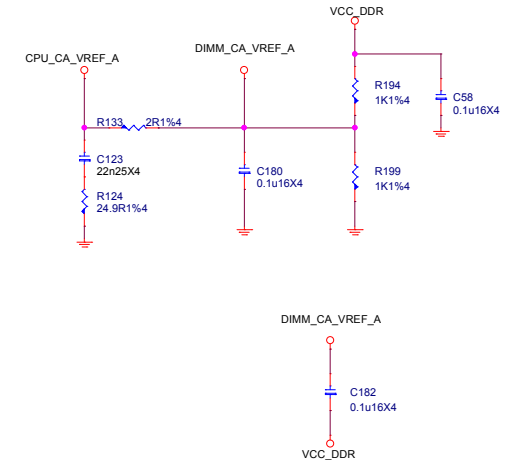
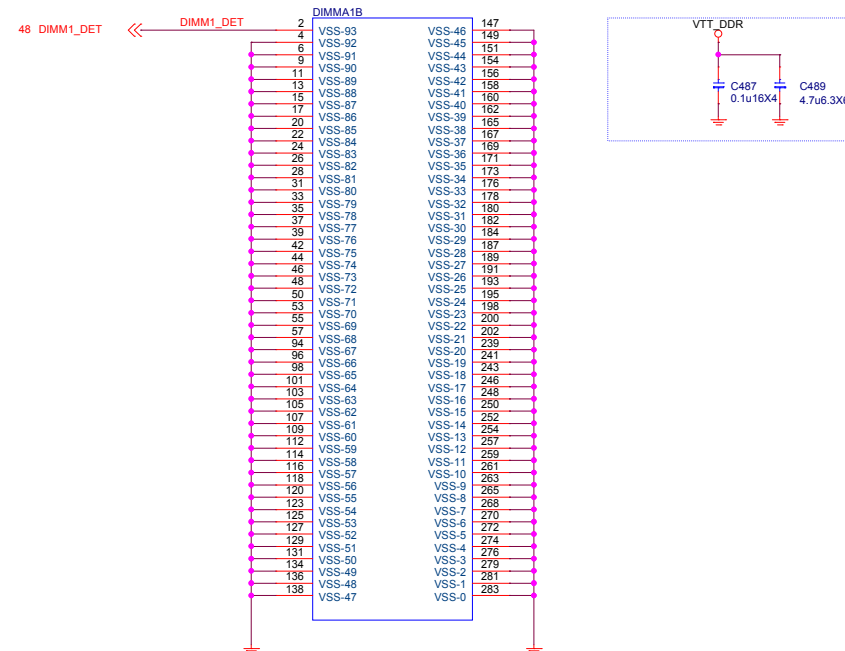


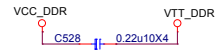
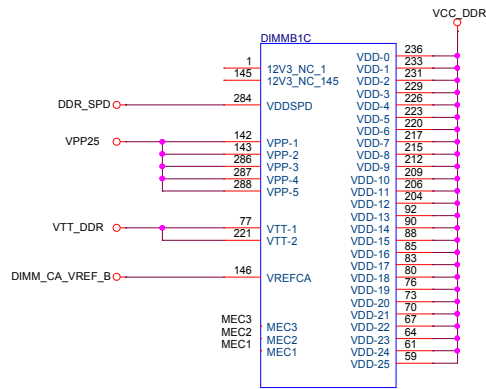




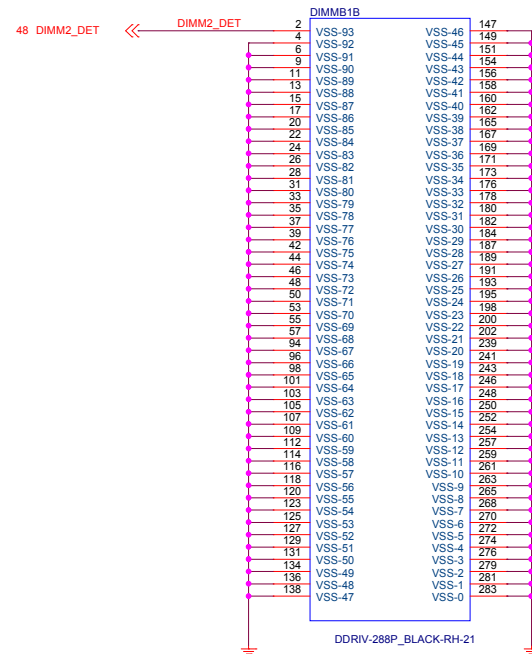
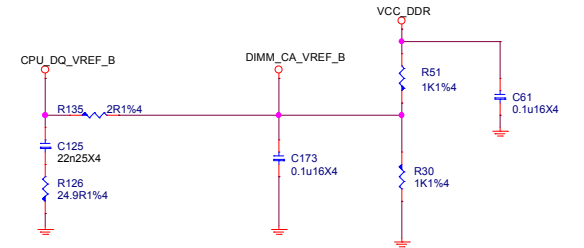
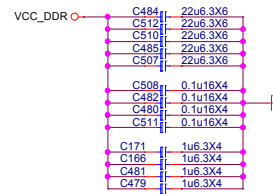
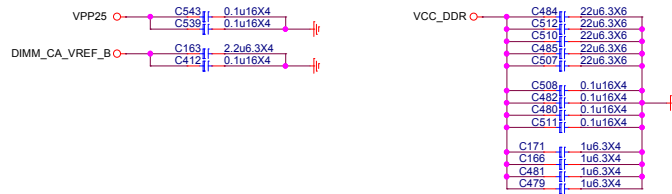


0.1uFx1 per dimm

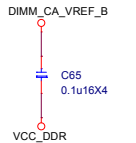
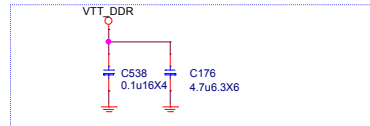


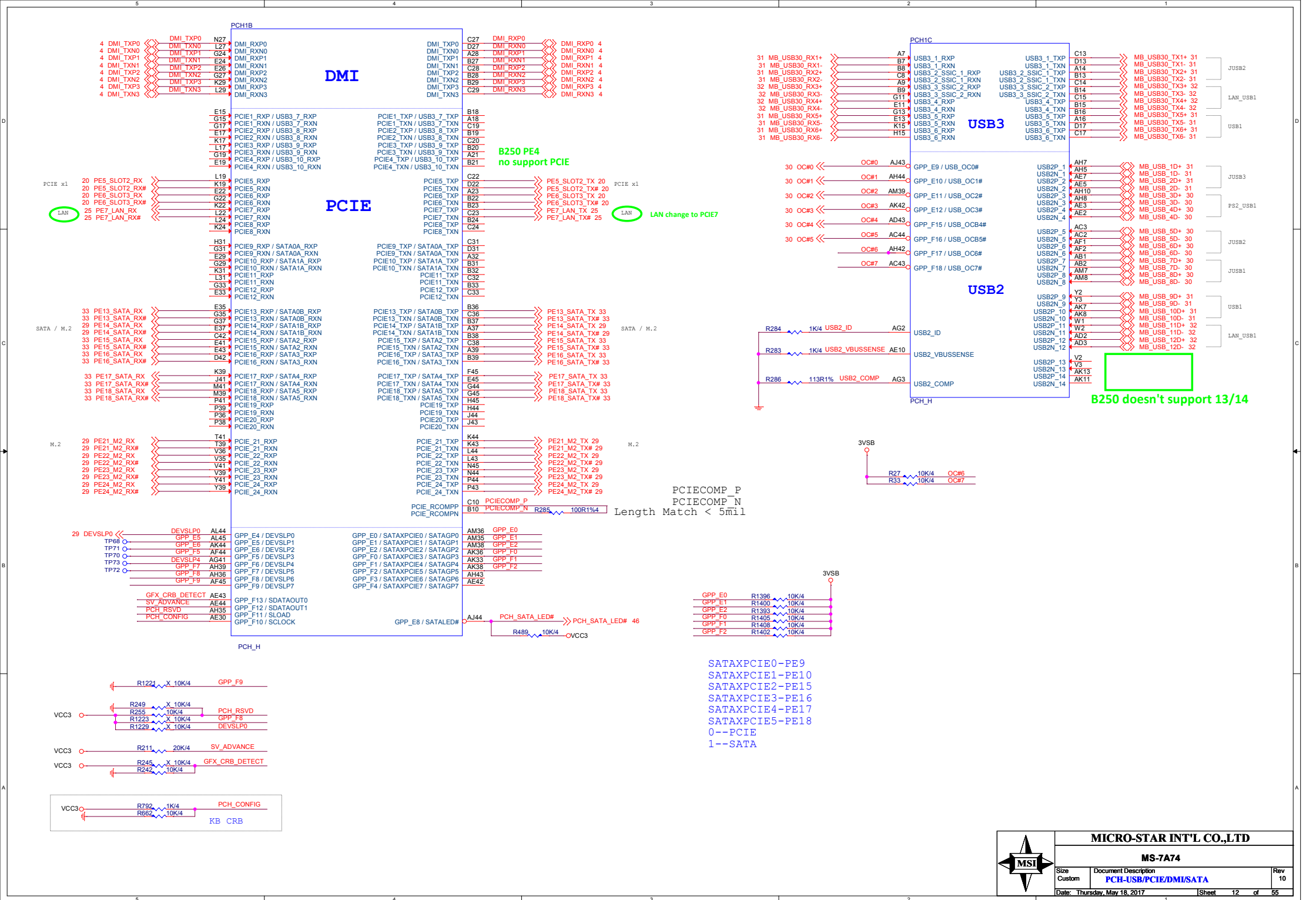


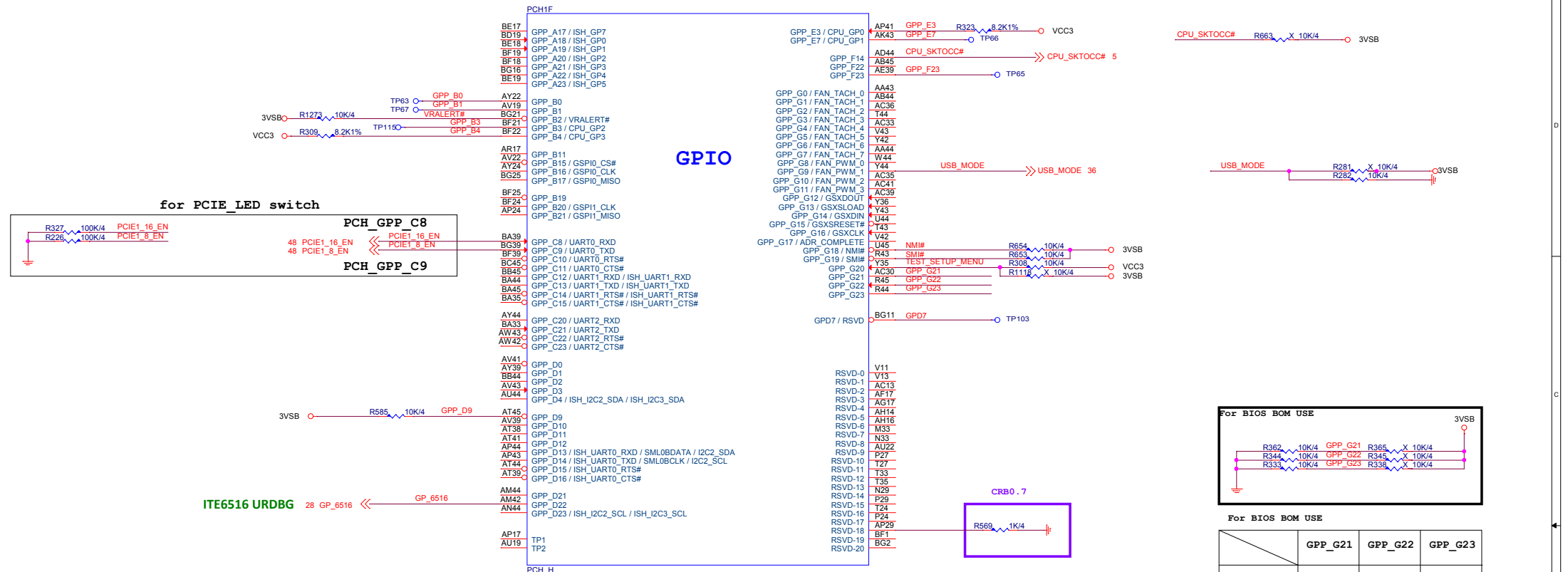
Place close to DIMM2



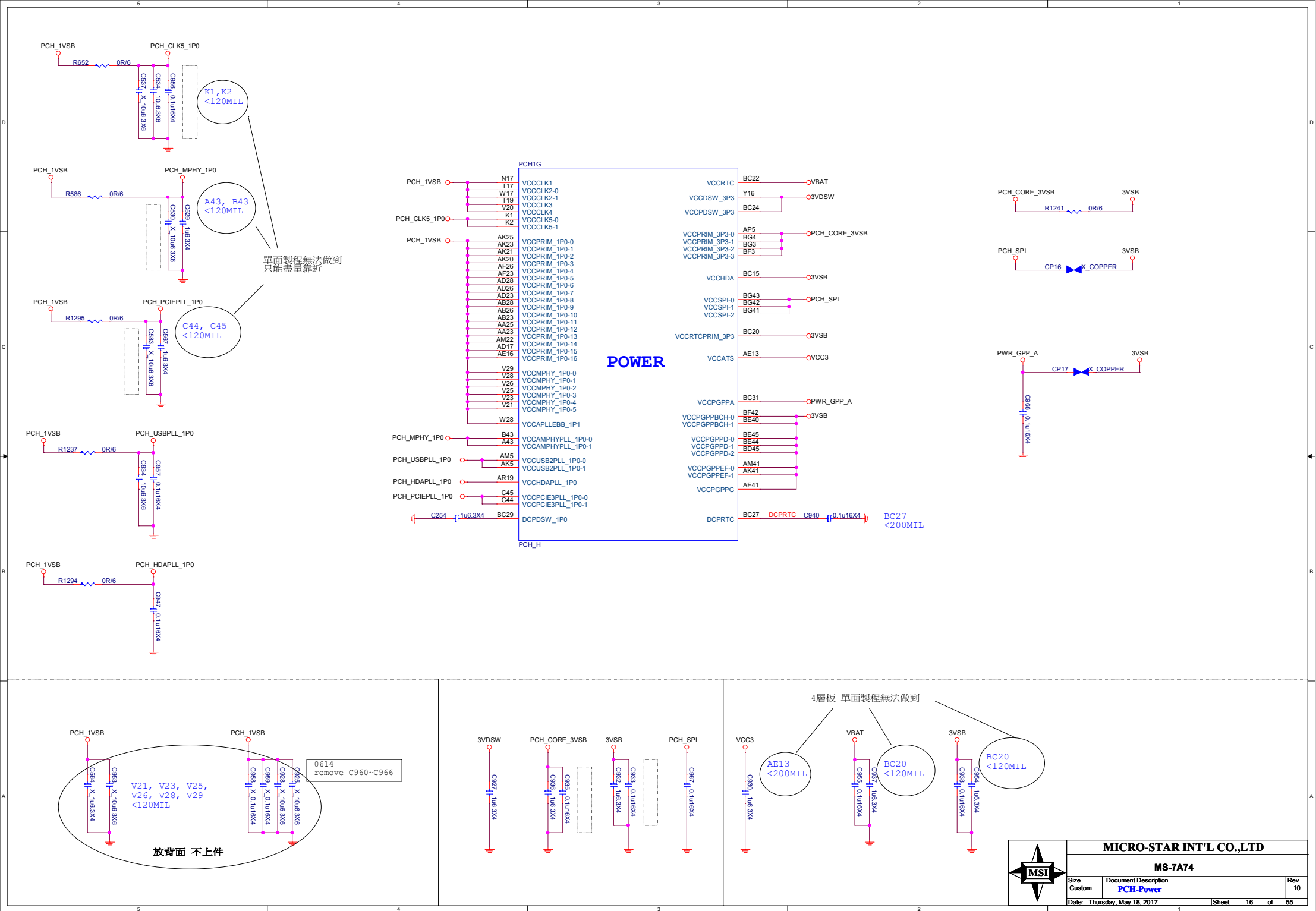
0.1uFx1 per dimm







	GPP_G21	GPP_G22	GPP_G23
B250M PRO-VH	0	0	0
B250M PRO-VD	0	0	1
B250M NANO	0	1	0
B250M ICAFE	0	1	1
B250M-D	1	0	0
B250M-E	1	0	1
B250M-F	1	1	0
B250M G1 GAMER	1	1	1



VSS

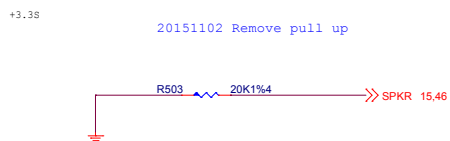


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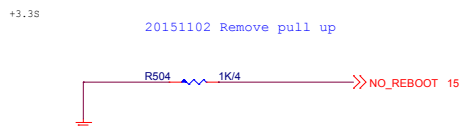
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TOP Swap



Internal pull-down 20K is disabled after PLTRST#

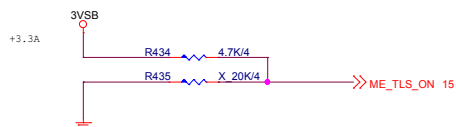
No Reboot



0 : DISABLE (Default)
1 : ENABLE

Internal pull-down 20K is disabled after PLTRST#

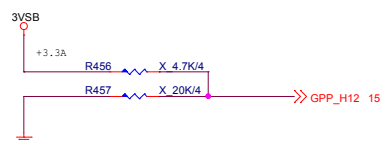
AMT and SBA with confidentiality



0 : DISABLE
1 : ENABLE (Default)

Internal pull-down 20K is disabled after RSMRST

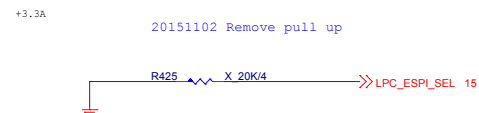
ESPI FLASH SHARING MODE



0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

Internal pull-down 20K is disabled after RSMRST

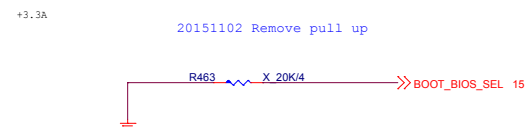
LPC eSPI Mode



0 : LPC
1 : eSPI

Internal pull-down 20K is disabled after RSMRST

Boot BIOS

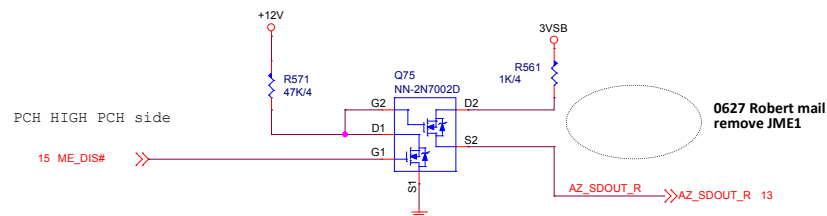


0 : SPI
1 : LPC

Internal pull-down 20K is disabled after PLTRST

HDA_SDO

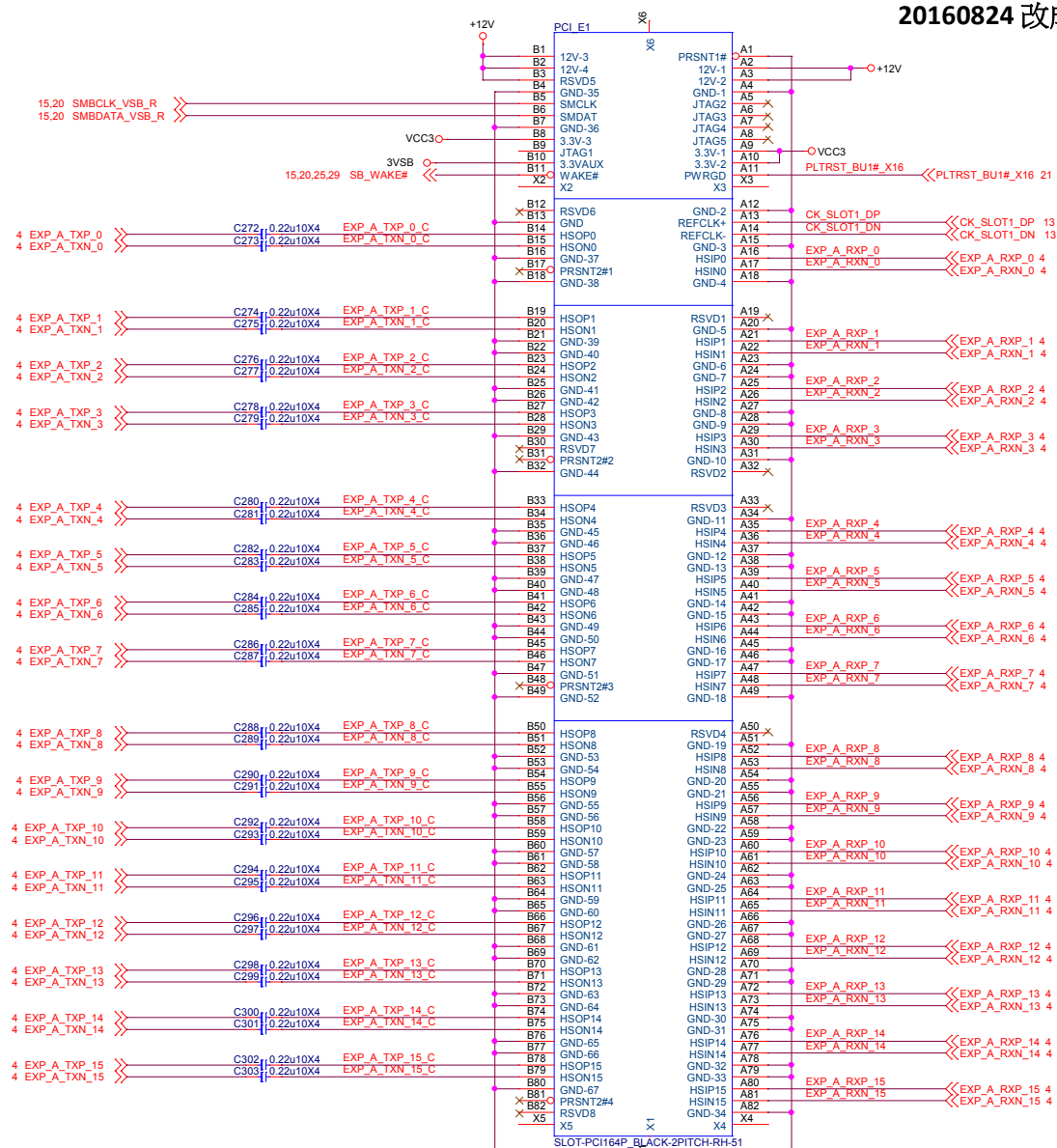
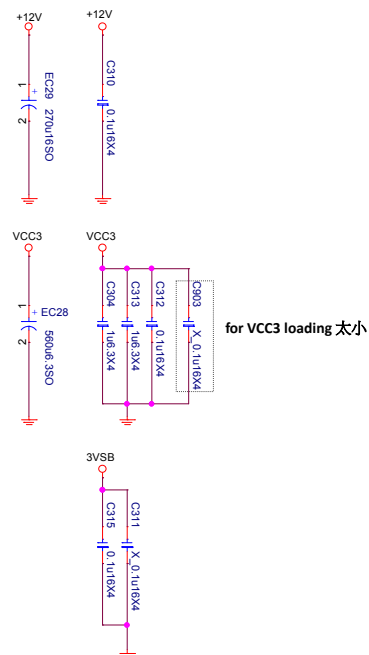
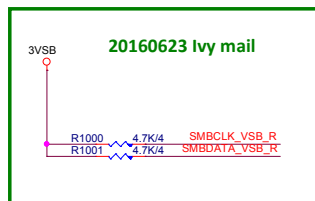
ME flash by GPIO

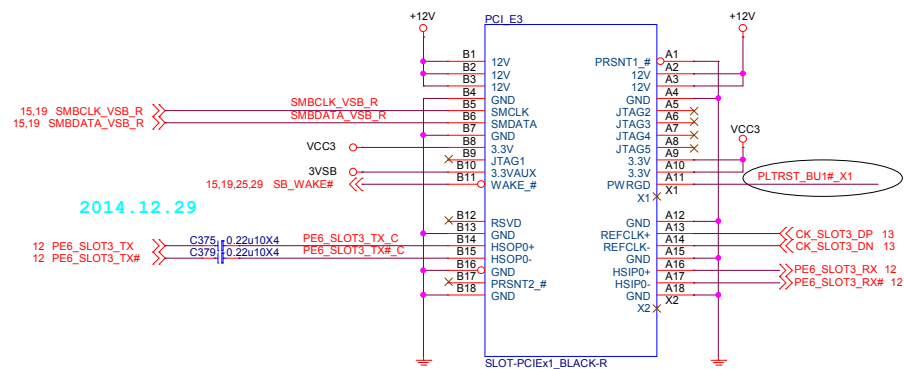
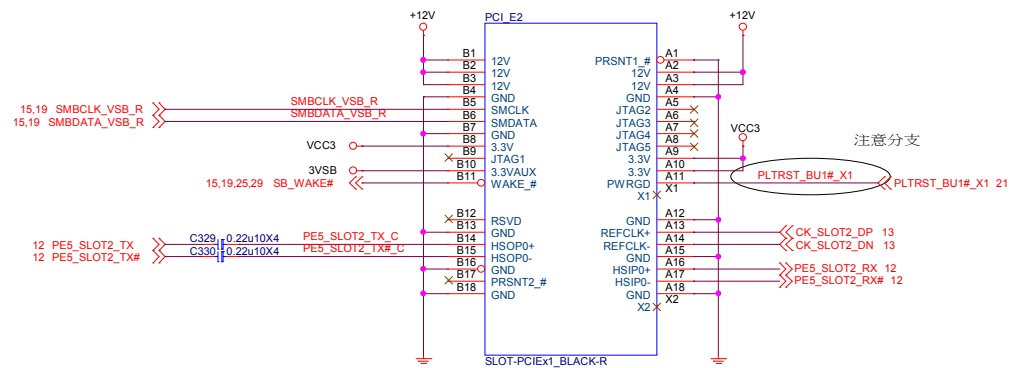


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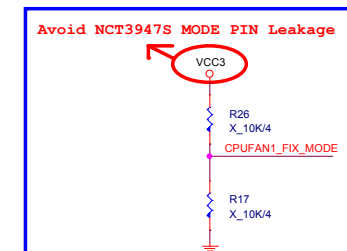
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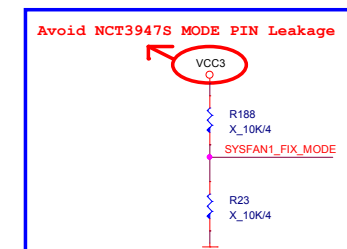




2. GPIO可以由BIOS切換 PWM/DC MODE



2.GPIO可以由BIOS切換 PWM/DC MODE

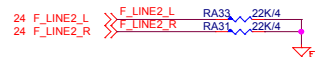
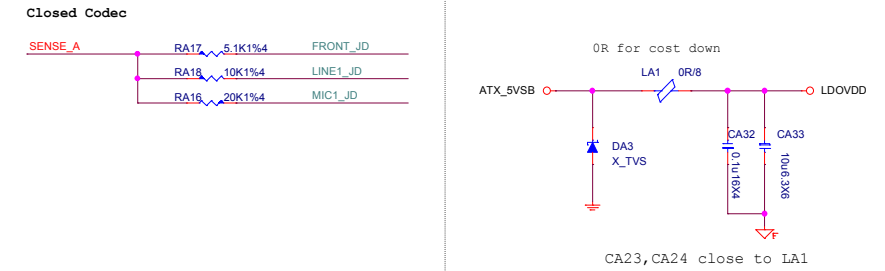
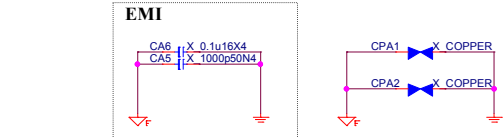
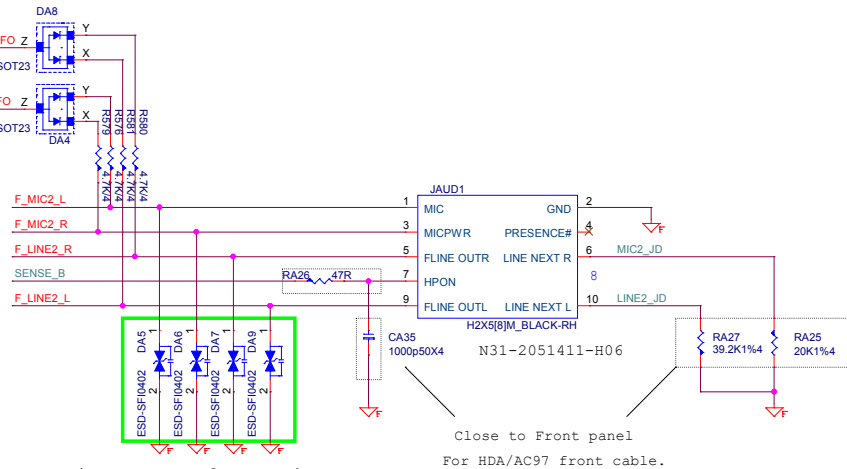
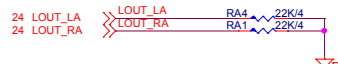
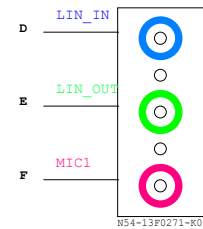
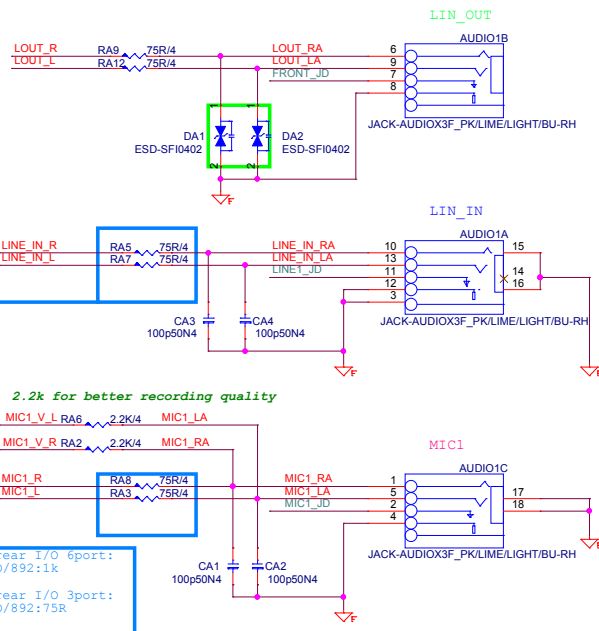
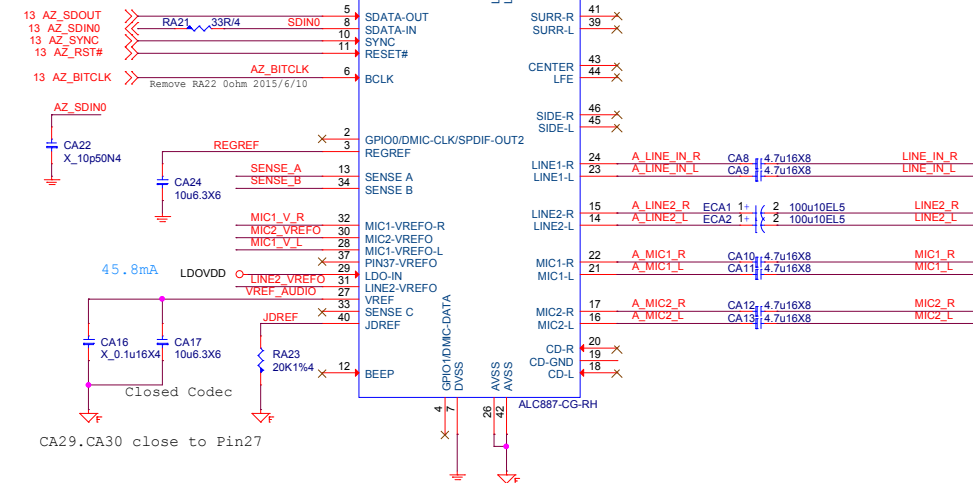


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Type B: ALC892/887

Closed code 2015/6/22

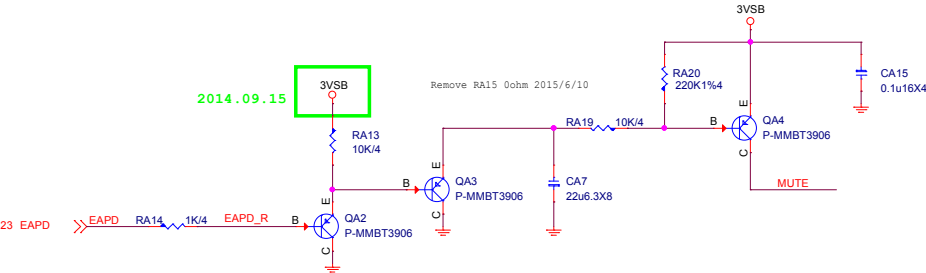


Varister --> cap for cost down
D0G-2950500-SI0
D0G-3010510-I05
Close to Jack

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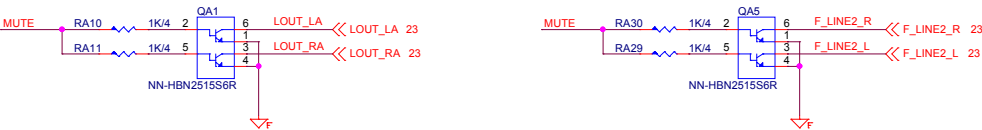
Rear Line OUT De-POP circuit

De-pop circuit for Rear Line out & Front Headphone out)

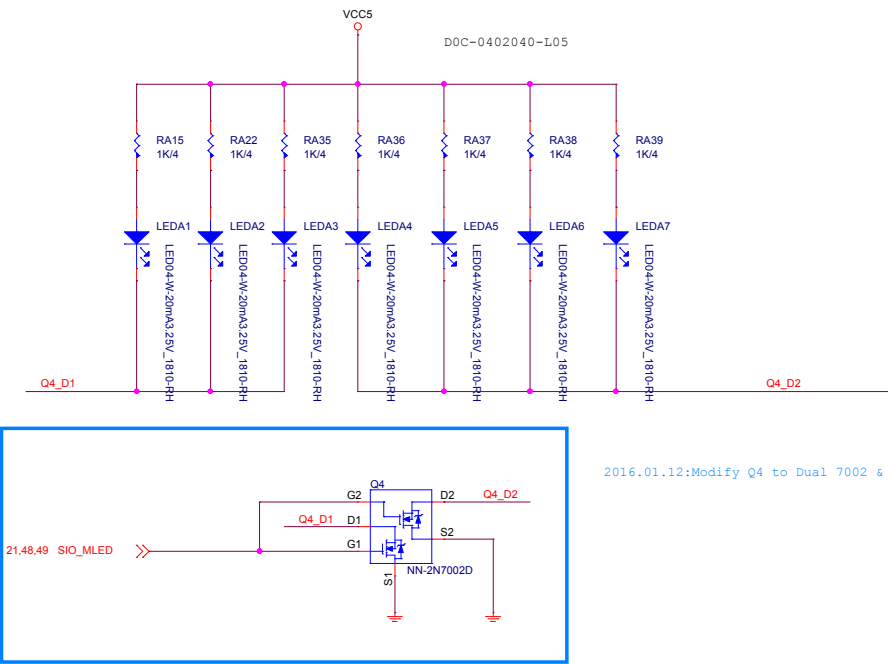


Digital

Analog



Audio LED



2016.01.12:Modify Q4 to Dual 7002 & Remove OR

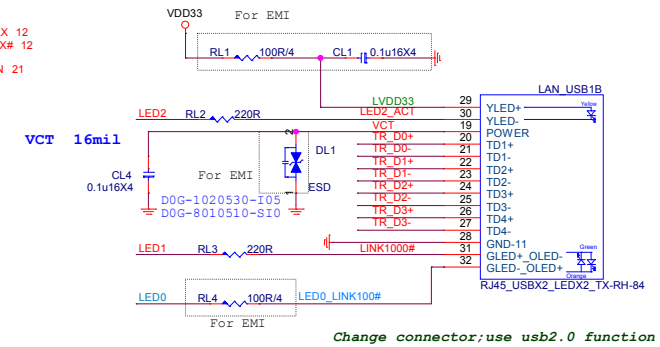
RTL8111G/RTL8111H Giga LAN

8111H:B06-08111CC-R09
8111G:B06-081116C-R09

2016.08.26 崑山反應

LAN_CLKREQ#4_R R1014 0R/4 LAN_CLKREQ#4 13

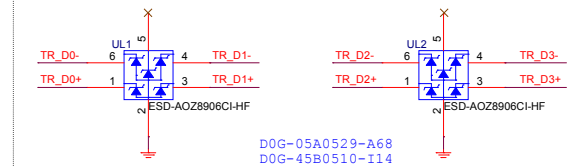
LAN Connector



Pin33: 4 via from top layer to GND layer and make the via at the center of IC.

ESD Protect

UL1 & UL2 close to connector



8111G POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDFS	6.41	21.15

8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDFS	5.50	18.15

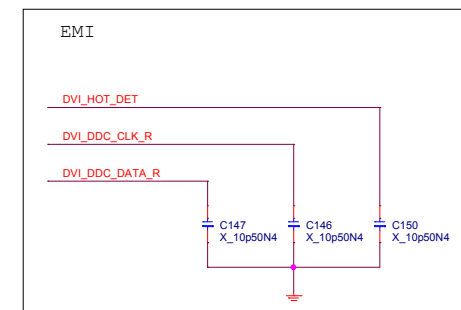
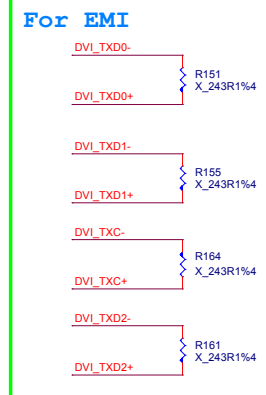
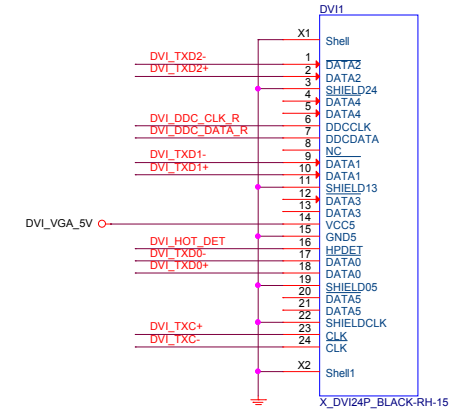


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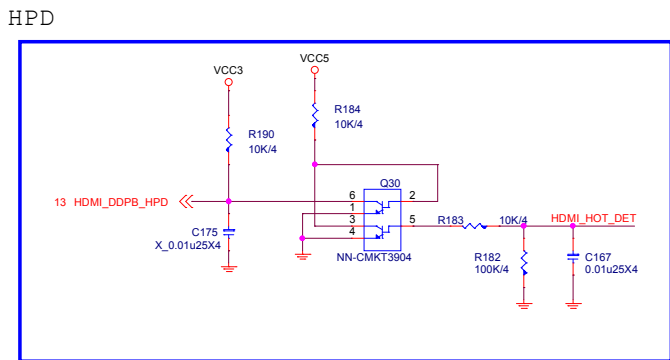
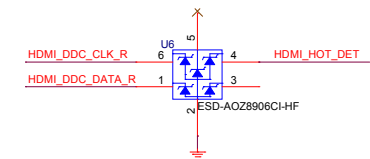
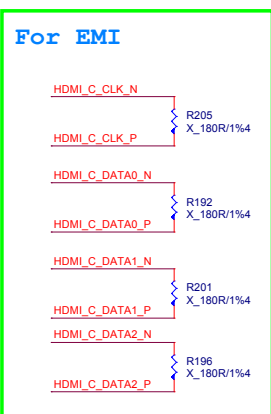
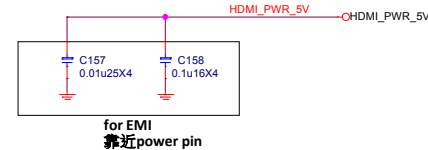
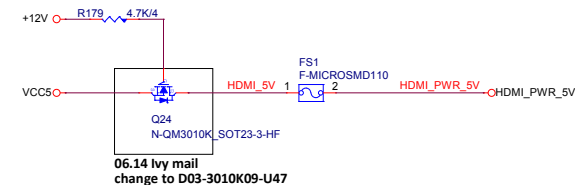
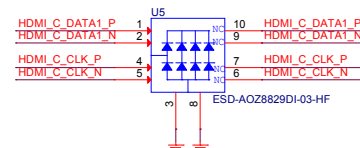
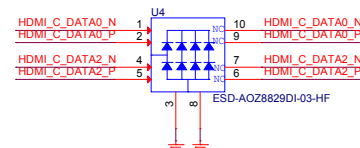
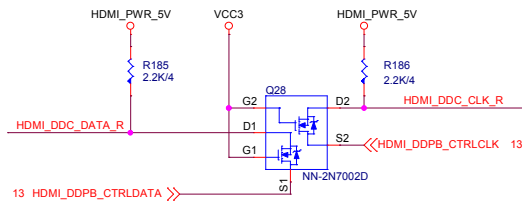
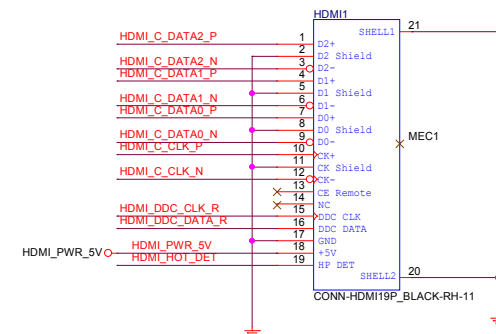
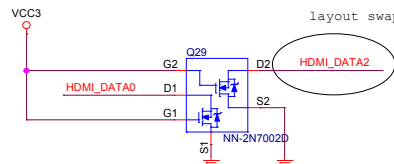
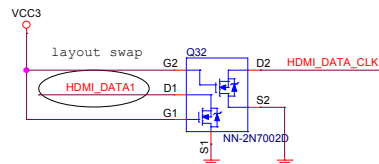
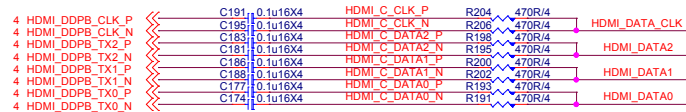
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



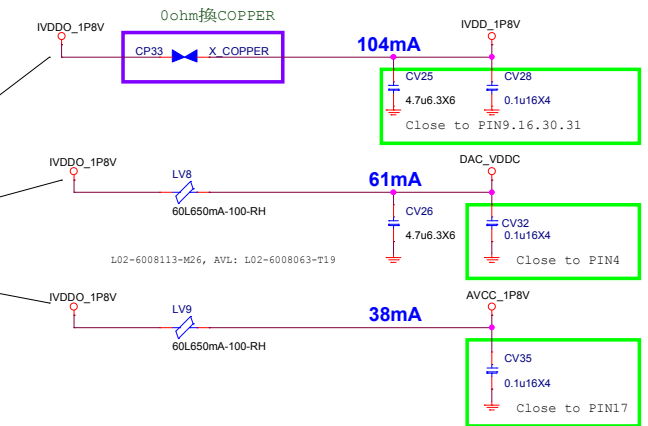
MS-7A74

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Date: Thursday, May 18, 2017		Sheet 26 of 55

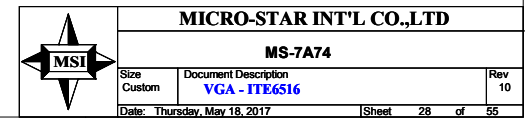
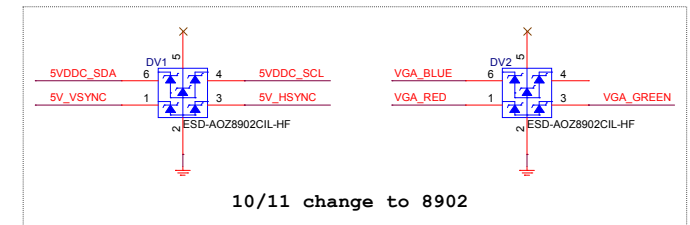
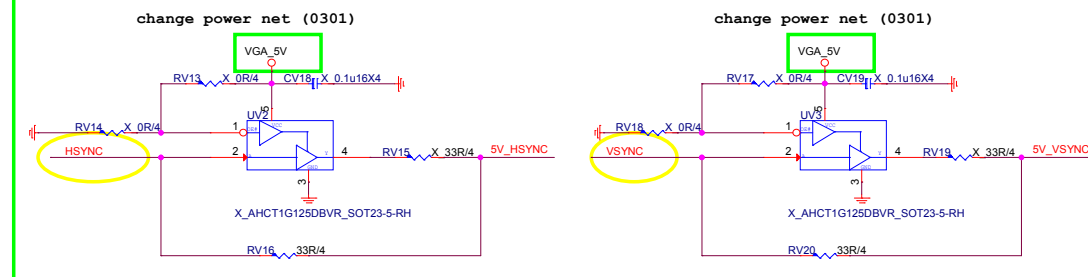
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)

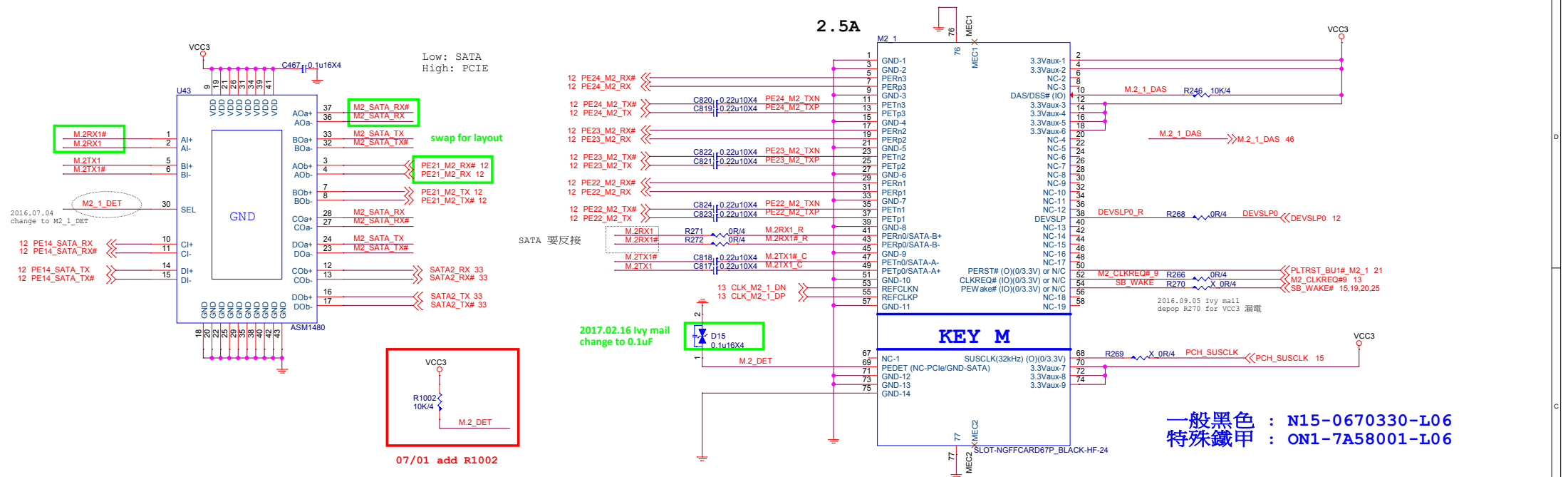


If connect to eDP port, must confirm whether it support hot plug detection HPD and re-auxtraining



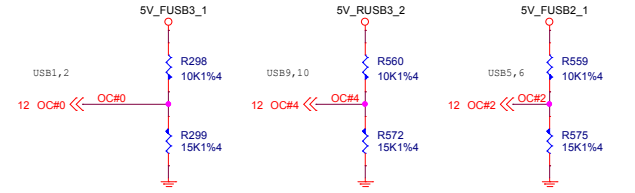
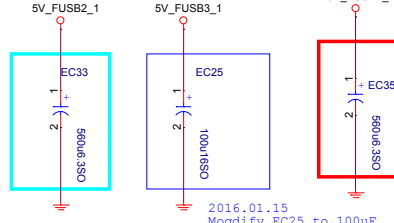
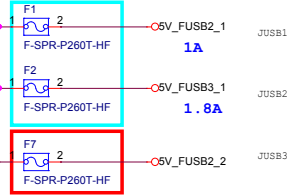
System Status	GPIO	IT6516b's HPD
Legacy Mode (VBIOS) /DOS Mode	HIGH	Force HIGH
Windows /UEFI Mode (GOP)	LOW	Depend on VGA device's plug/unplug



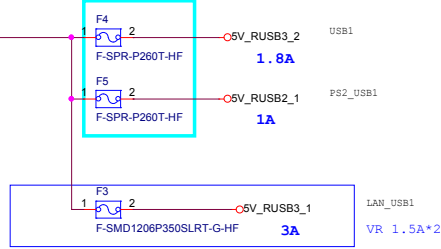


20151105 Modify to 5VDIMM

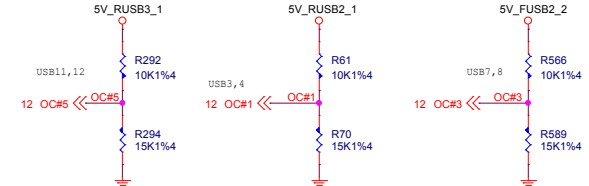
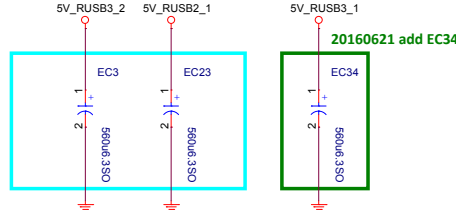
20150317 change to IVY mail



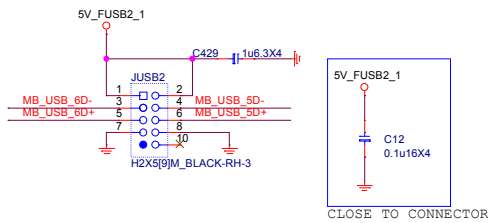
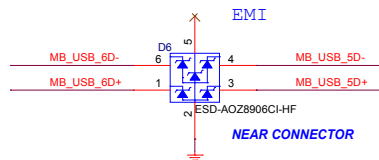
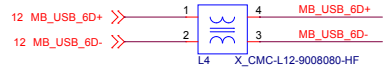
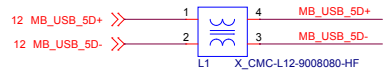
20150317 change to IVY mail



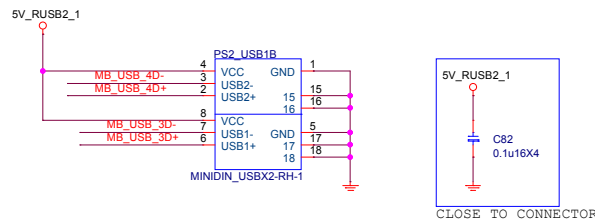
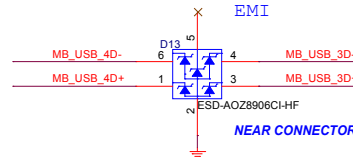
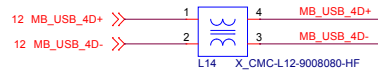
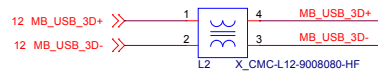
20150924 change USB CAP



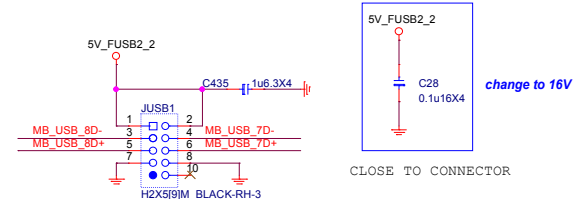
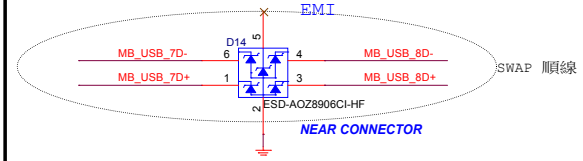
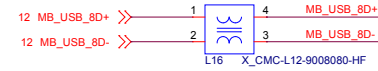
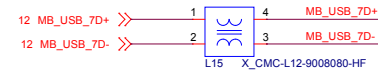
FRONT JUSB2 PORT 5,6



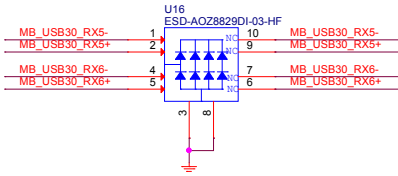
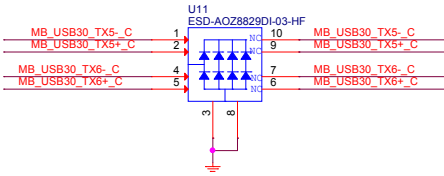
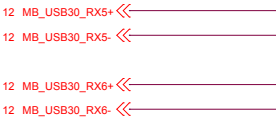
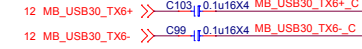
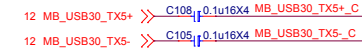
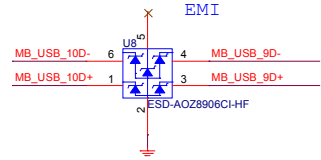
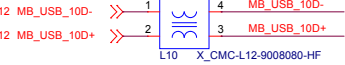
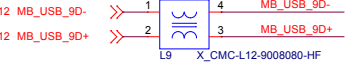
PS2_USB1 PORT 3,4



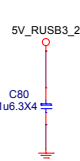
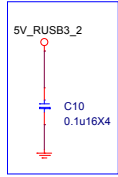
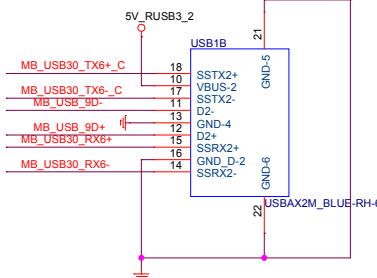
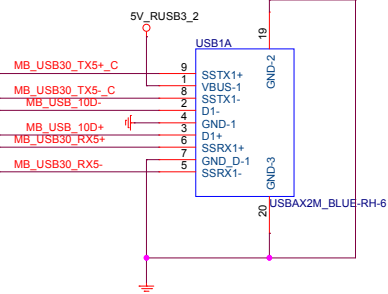
FRONT JUSB1 PORT 7,8



Rear USB1 port 9,10

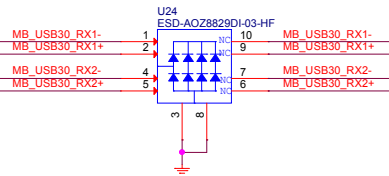
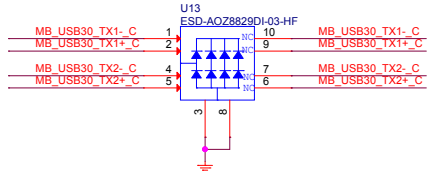
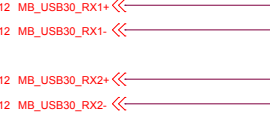
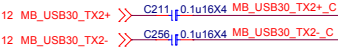
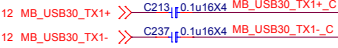
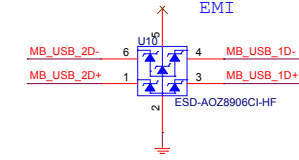
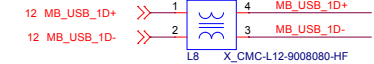
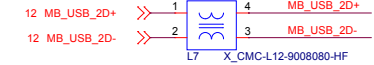


10/06 change to GF

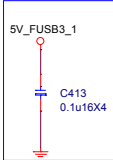
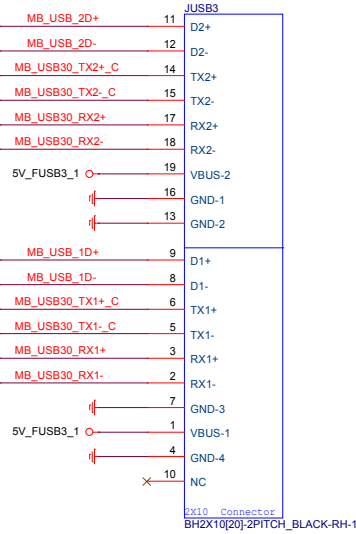


CLOSE TO CONNECTOR

Front JUSB3 port 1,2



10/06 change to N32-2101091-H06

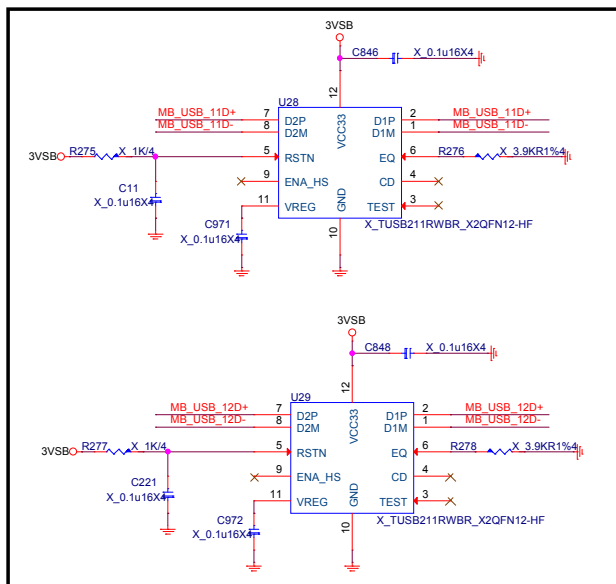
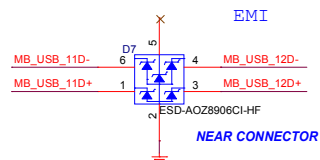
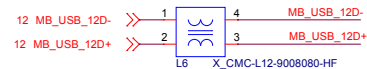
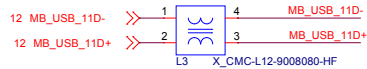


CLOSE TO CONNECTOR



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Size	Document Description	Rev	
Custom	Rear USB3 & Front Connector	10	
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LAN_USB port 11,12



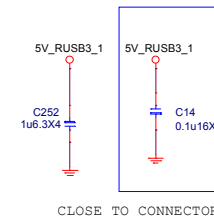
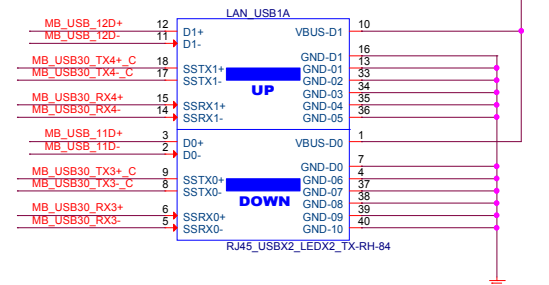
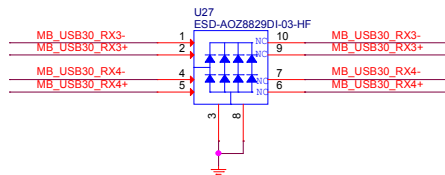
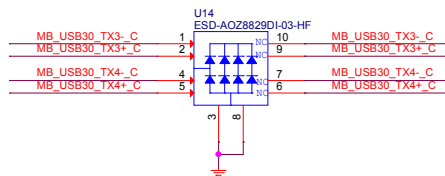
2016.05.30 PM add VR function
2016.09.23 remove VR

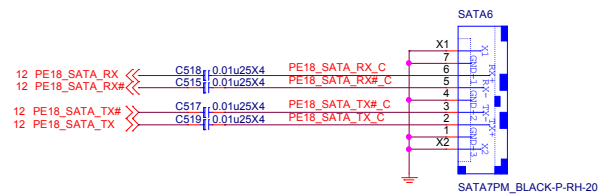
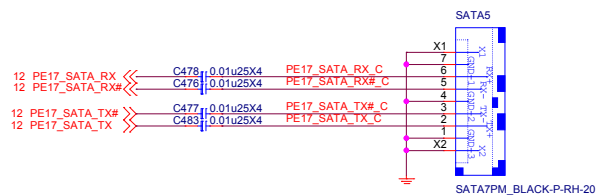
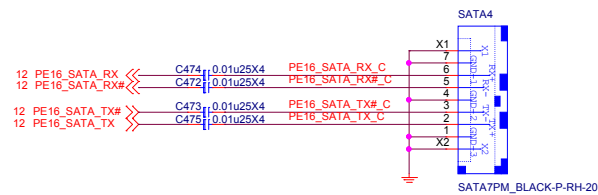
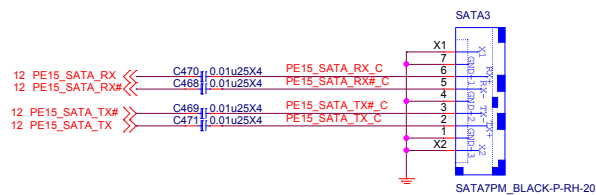
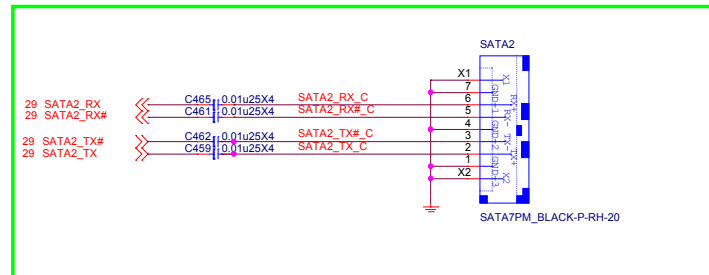
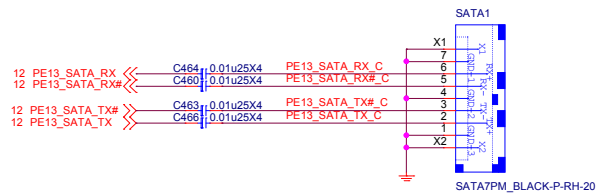
12 MB_USB30_TX3+ >> C133 0.1u16X4 MB_USB30_TX3+_C
12 MB_USB30_TX3- >> C151 0.1u16X4 MB_USB30_TX3-_C

12 MB_USB30_TX4+ >> C128 0.1u16X4 MB_USB30_TX4+_C
12 MB_USB30_TX4- >> C161 0.1u16X4 MB_USB30_TX4-_C

12 MB_USB30_RX3+ << MB_USB30_RX3+
12 MB_USB30_RX3- << MB_USB30_RX3-

12 MB_USB30_RX4+ << MB_USB30_RX4+
12 MB_USB30_RX4- << MB_USB30_RX4-



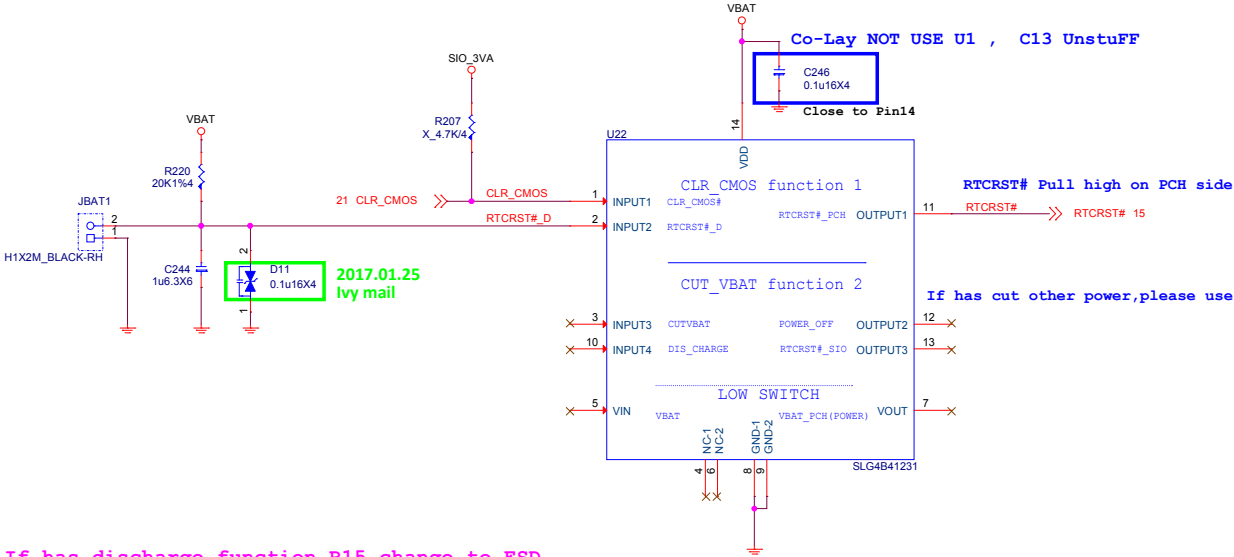
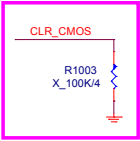


CLR_CMOS



If STUFF R20 Please Check RTCRST# Double Pull High

20160629

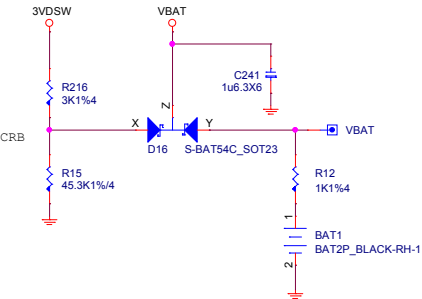


If has discharge function R15 change to ESD.
ESD"D0G-2950500-SI0"

Function 1		
IN		OUT
INPUT1	INPUT2	OUTPUT1
0	1	1
1	0	0
1	1	0
0	0	0

Default

VBAT



Function 2				
IN		OUT		
INPUT3 & lowswitch EN	INPUT4	OUTPUT2	OUTPUT3	VOUT
0	0	0	1	1
1	0	1	1	0 (discharge)
0	1	1	0	0 (discharge)
1	1	1	0	0 (discharge)

Default

Co-Lay NOT USE U1 , R20 STUFF

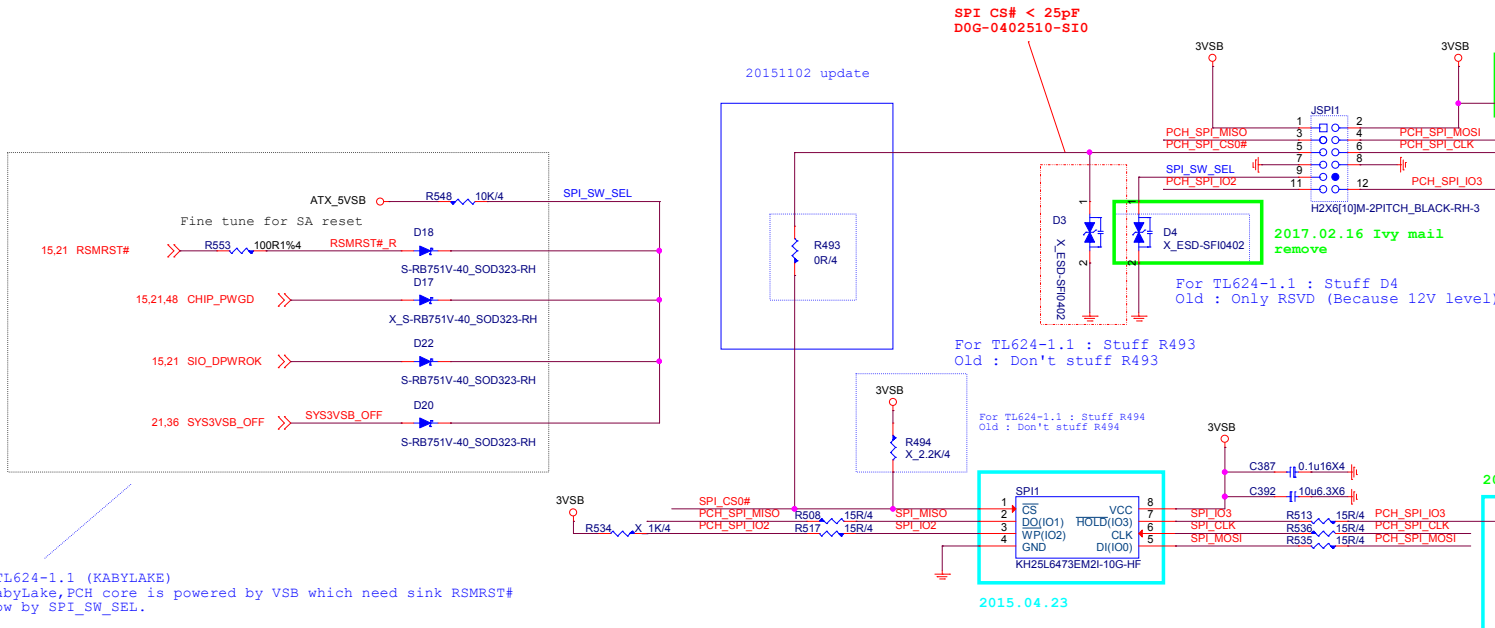


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15 PCH_SPI_MOSI << PCH_SPI_MOSI
15 PCH_SPI_MISO << PCH_SPI_MISO
15 PCH_SPI_CLK << PCH_SPI_CLK
15 PCH_SPI_CS0# << PCH_SPI_CS0#
15 PCH_SPI_IO2 << PCH_SPI_IO2
15 PCH_SPI_IO3 << PCH_SPI_IO3



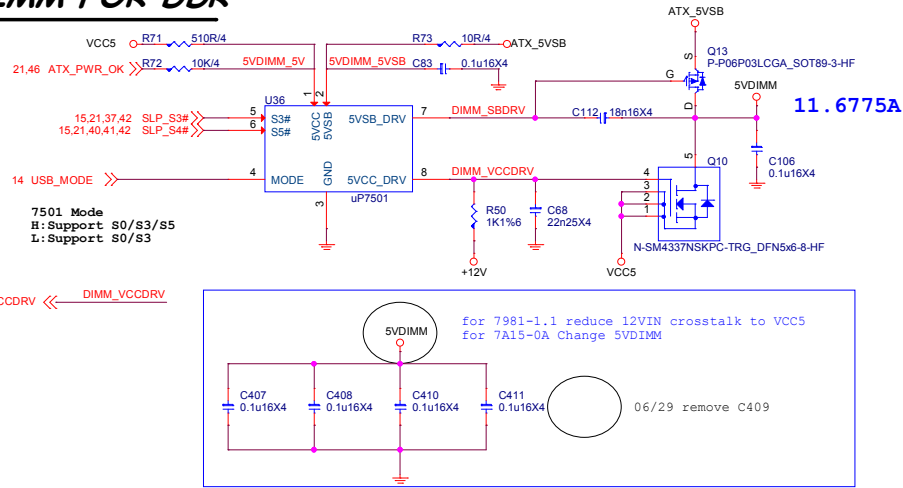
* if you not support Standby power in S5 Status, component Q14.G Pull-high to +12V & Q14 MOS select 2N7002

* if you support Standby power in S5 Status(Ex; PCH is B75 Chipset) , component Q14.G Pull-high to ATX_5VSB , Q14 must select "Vth" under 1V (Component Suggestion as below)

D03-0341409-A68 / D03-0230019-A30

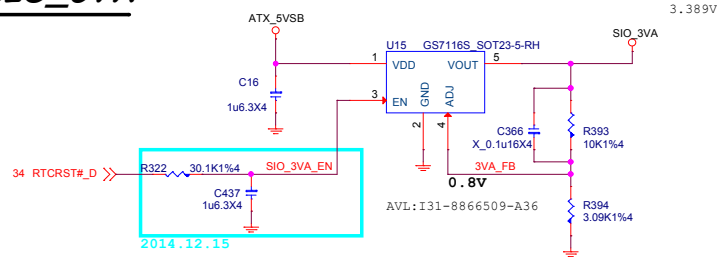
5VDIMM FOR DDR

(3A for DDR, 6.6A for USB)



SIO_3VA

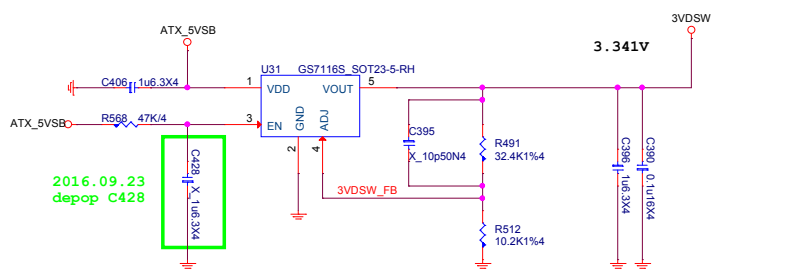
20mA



3VDSW

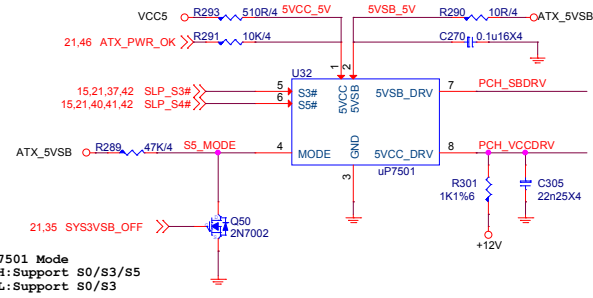
20151110 Modify to GS7116

204mA



5VDUAL

5VDUAL is power source of 1P0SB, 1.8PSB & 3VSB

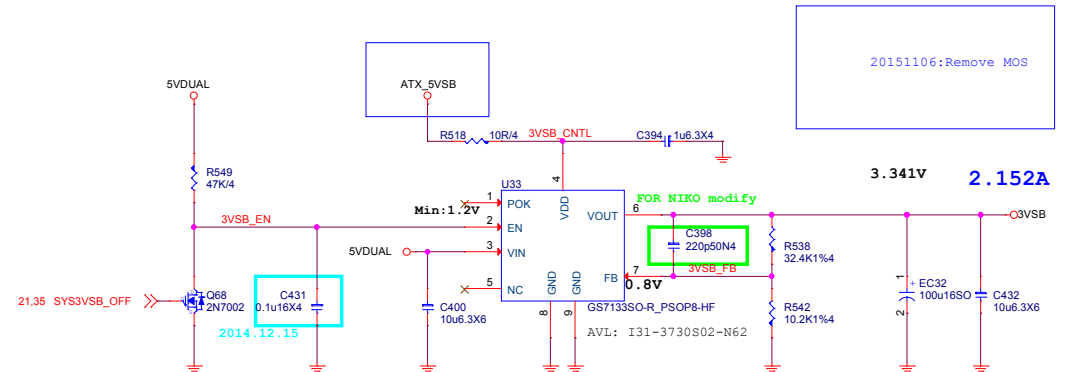


2015.09.15

For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 PCH VCCDRV work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.

20151106 :Remove 3VSB Patch Circuit

3VSB cost down

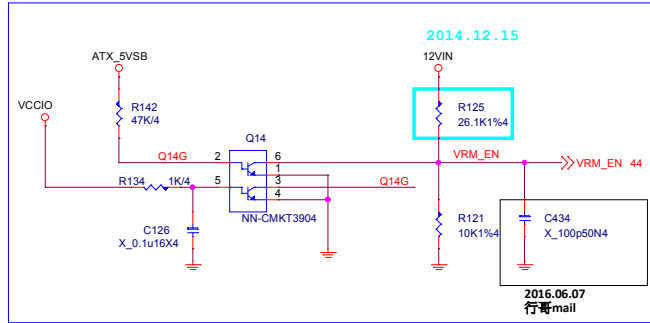


MICRO-STAR INT'L CO.,LTD

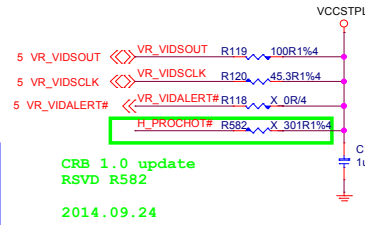
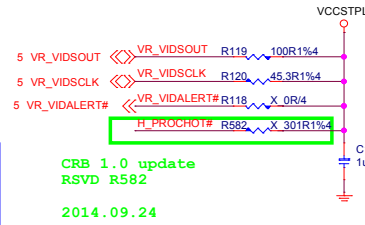
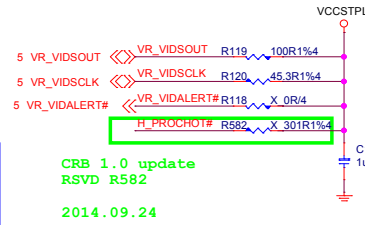
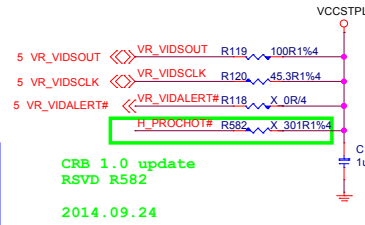
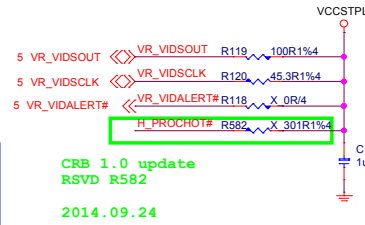
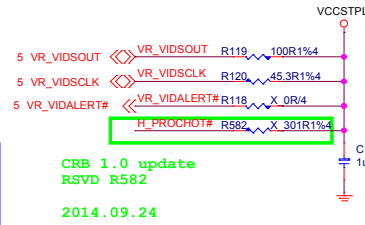
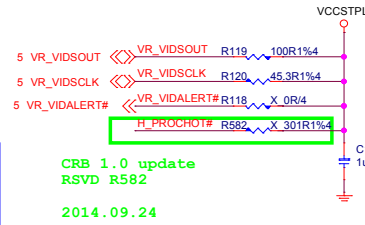
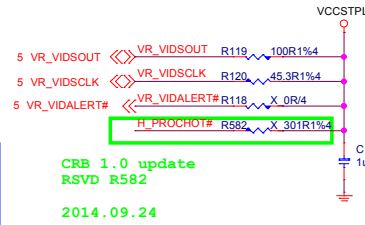
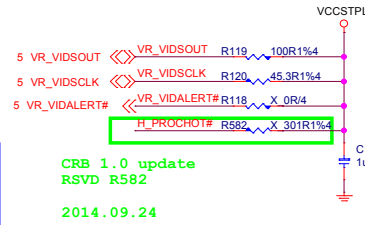
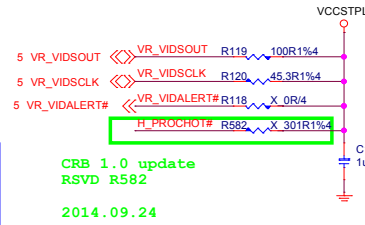
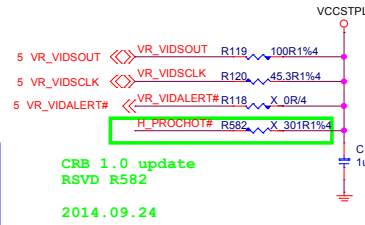
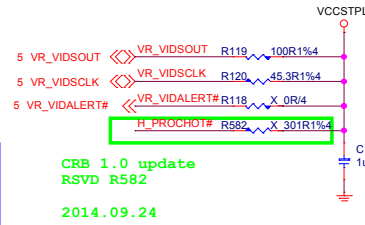
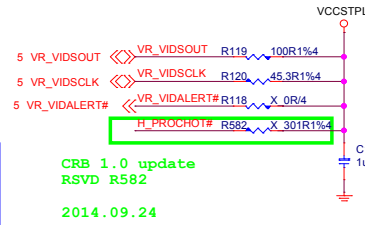
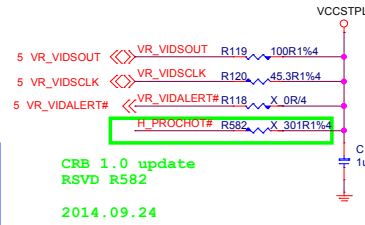
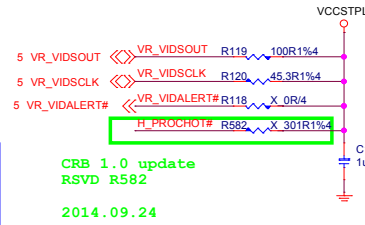
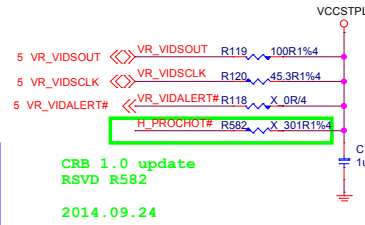
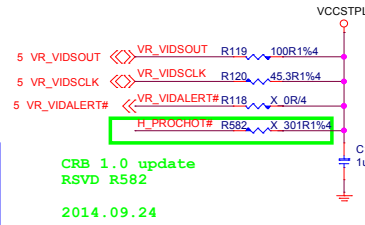
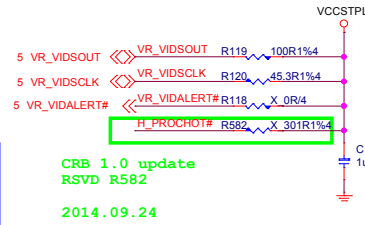
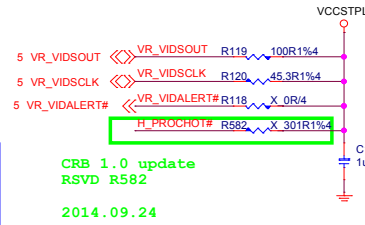
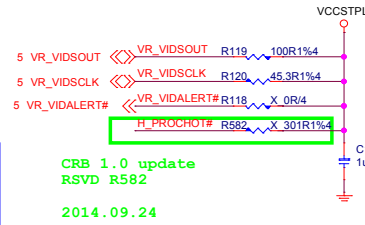
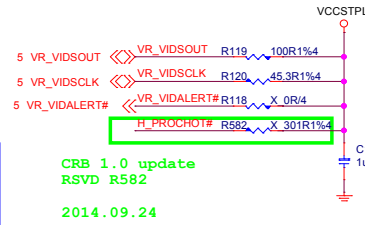
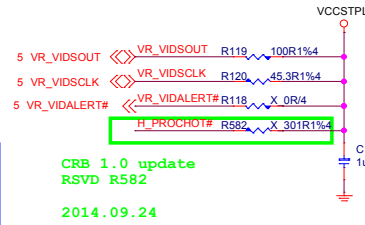
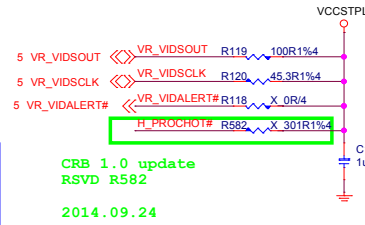
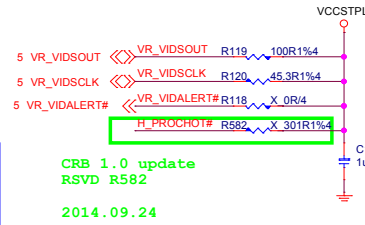
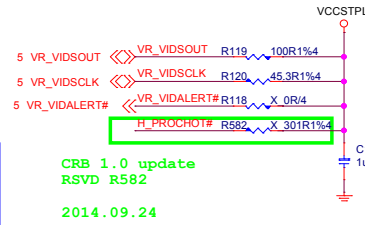
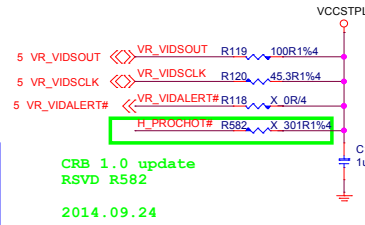
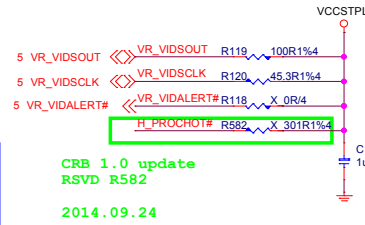
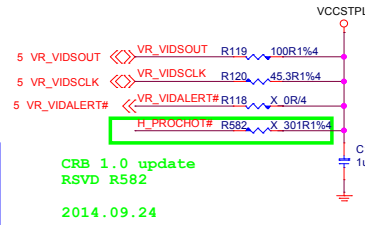
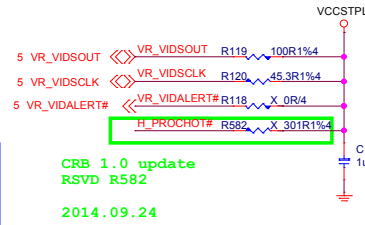
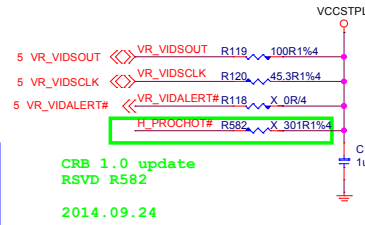
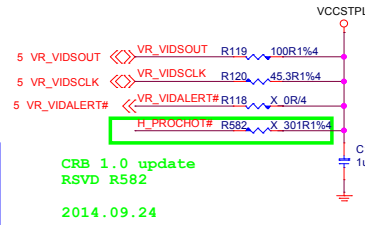
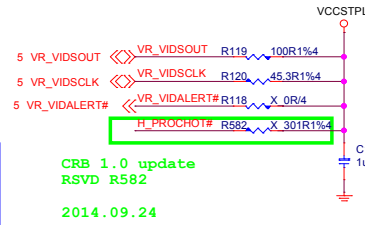
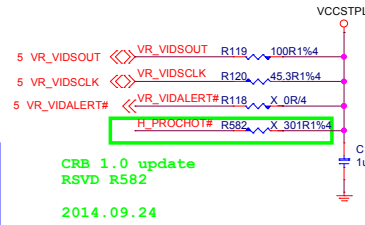
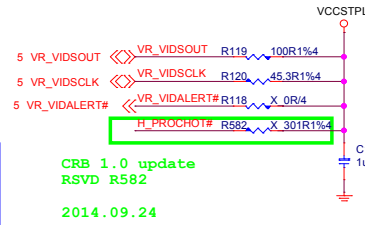
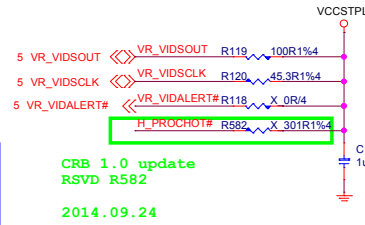
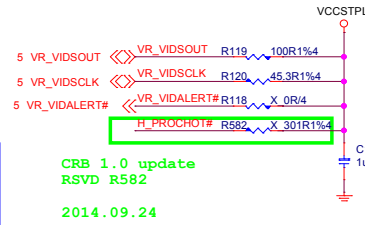
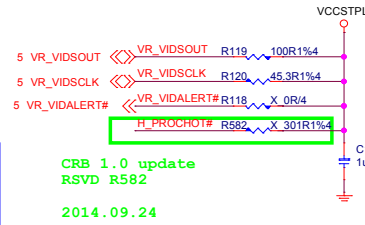
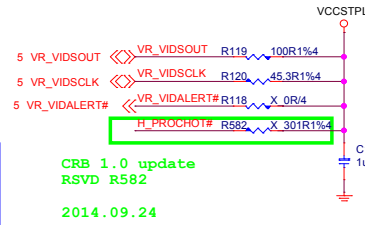
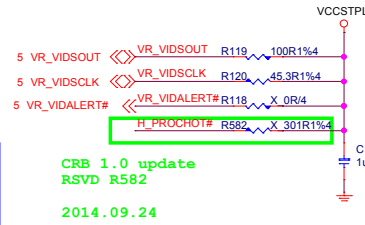
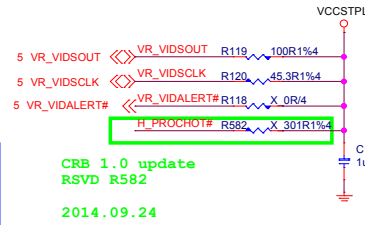
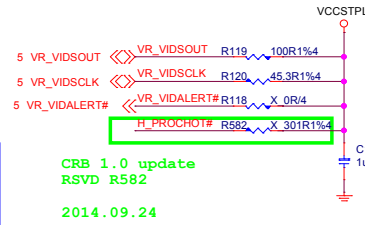
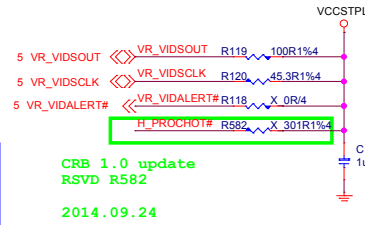
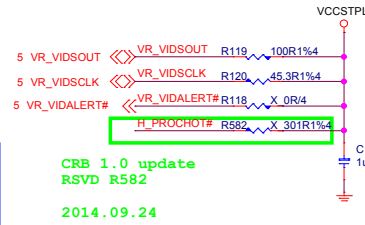
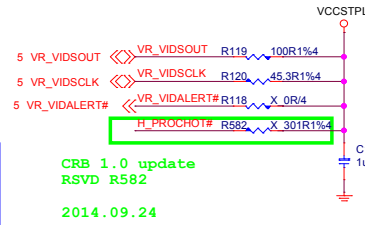
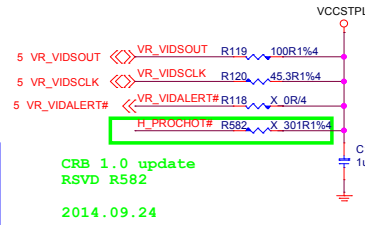
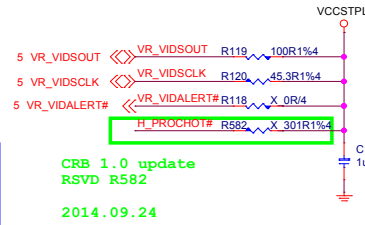
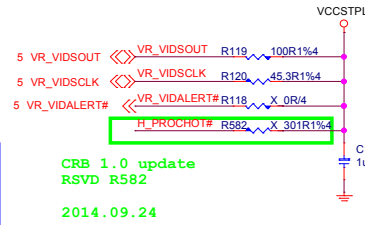
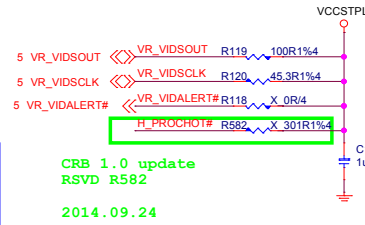
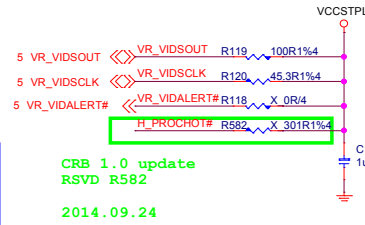
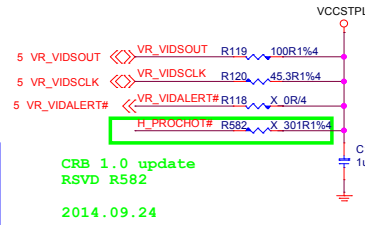
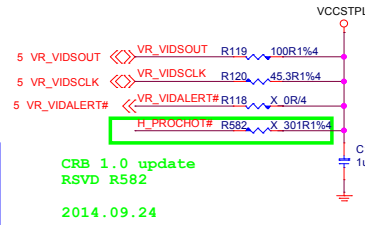
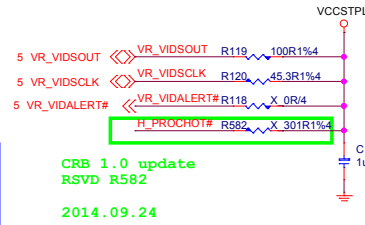
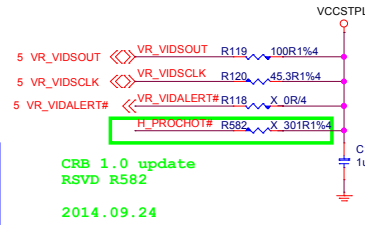
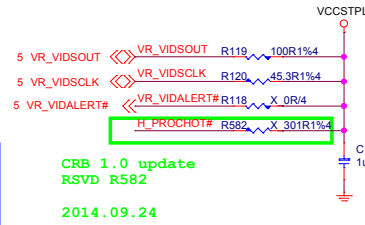
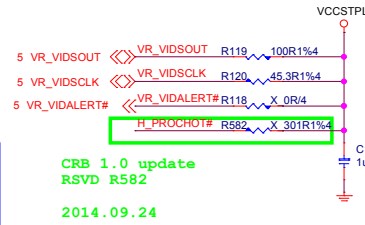
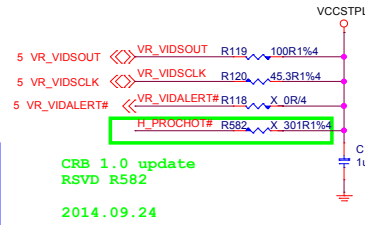
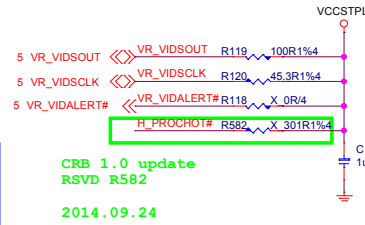
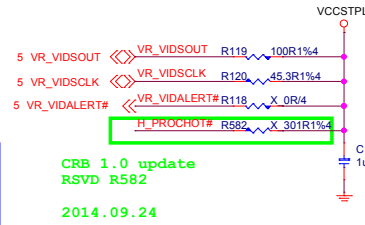
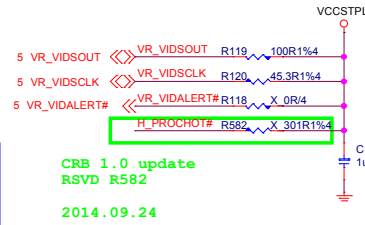
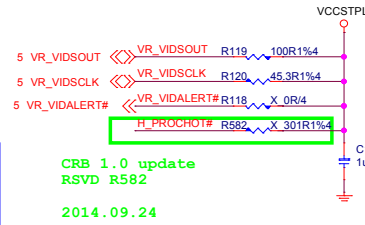
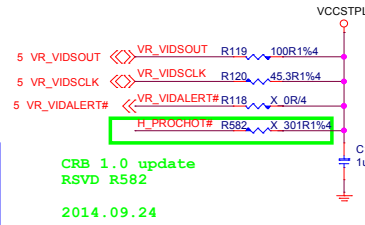
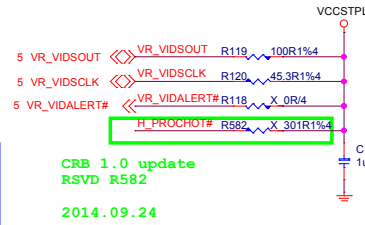
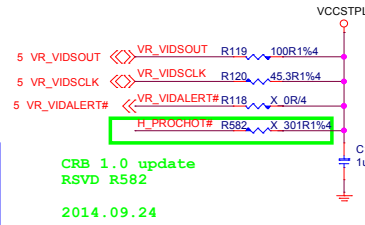
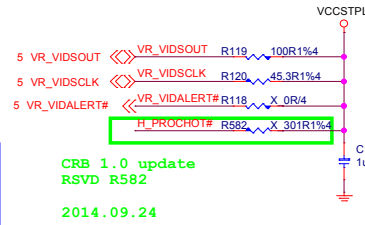
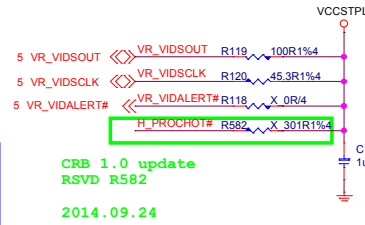
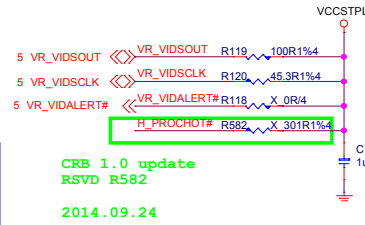
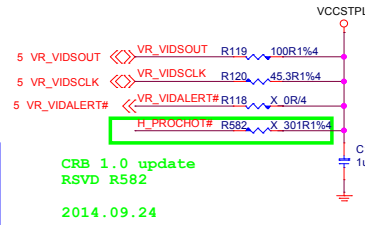
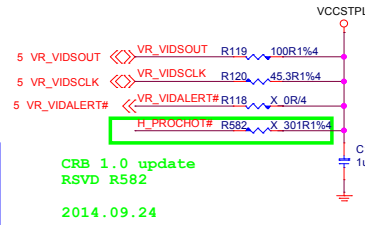
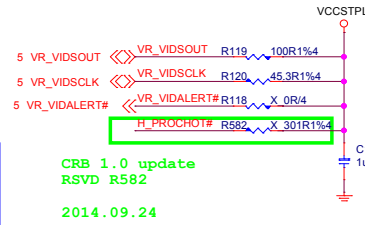
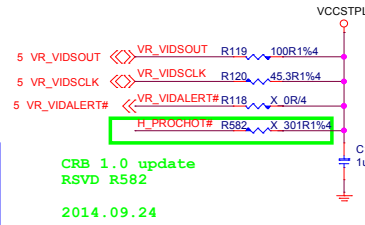
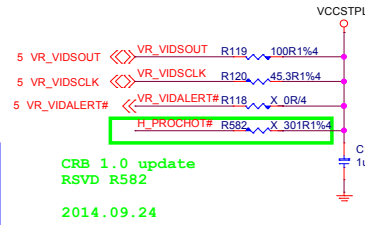
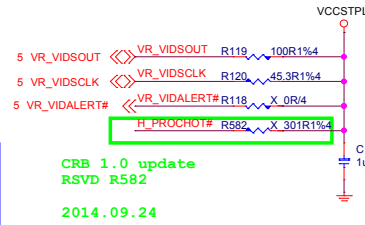
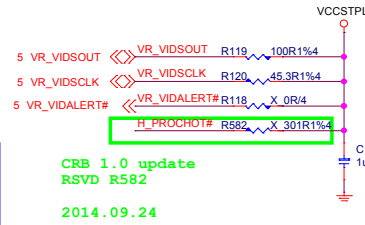
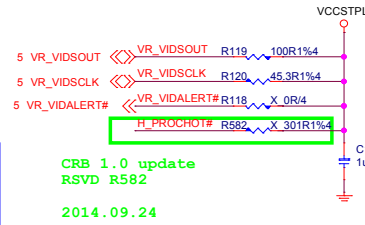
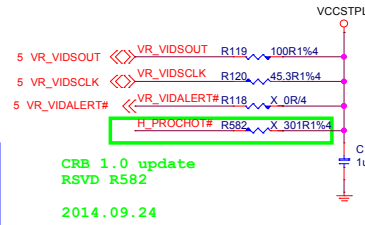
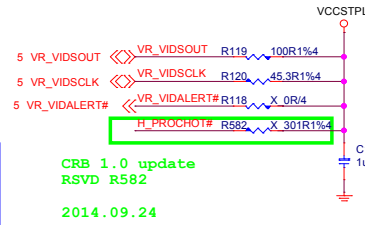
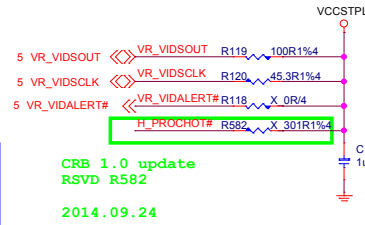
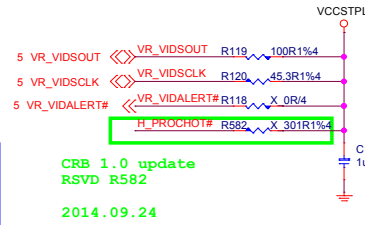
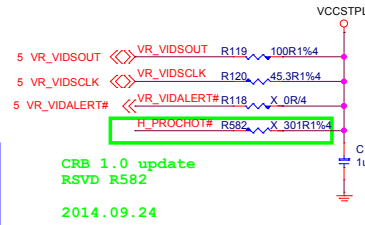
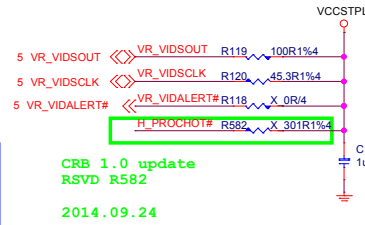
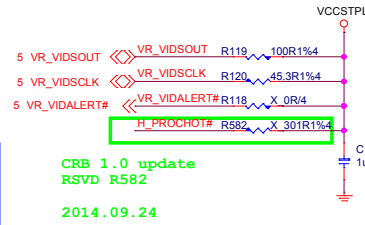
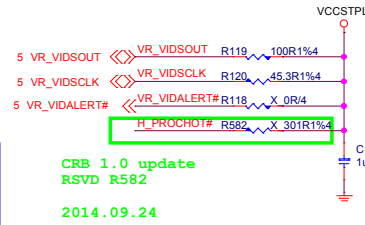
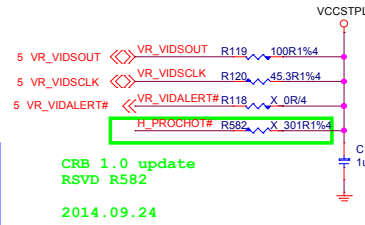
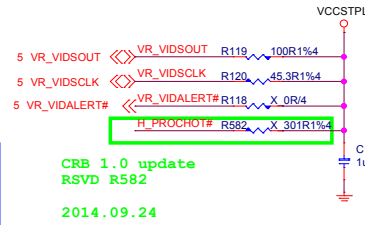
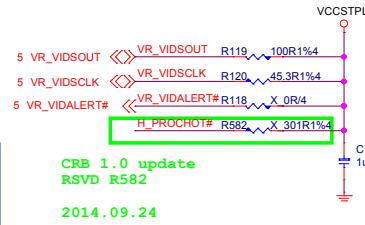
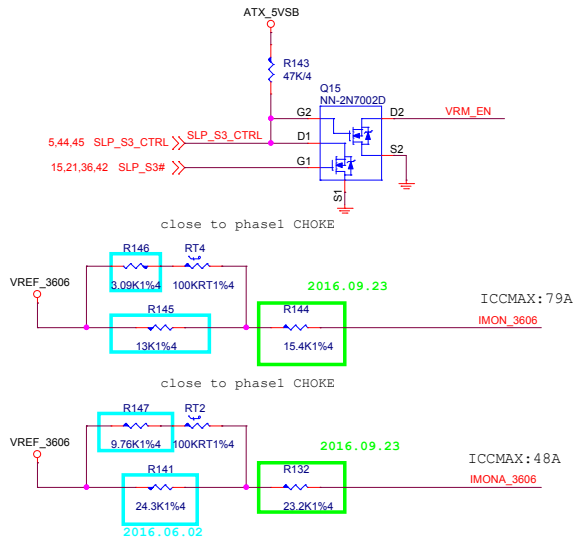
MS-7A74

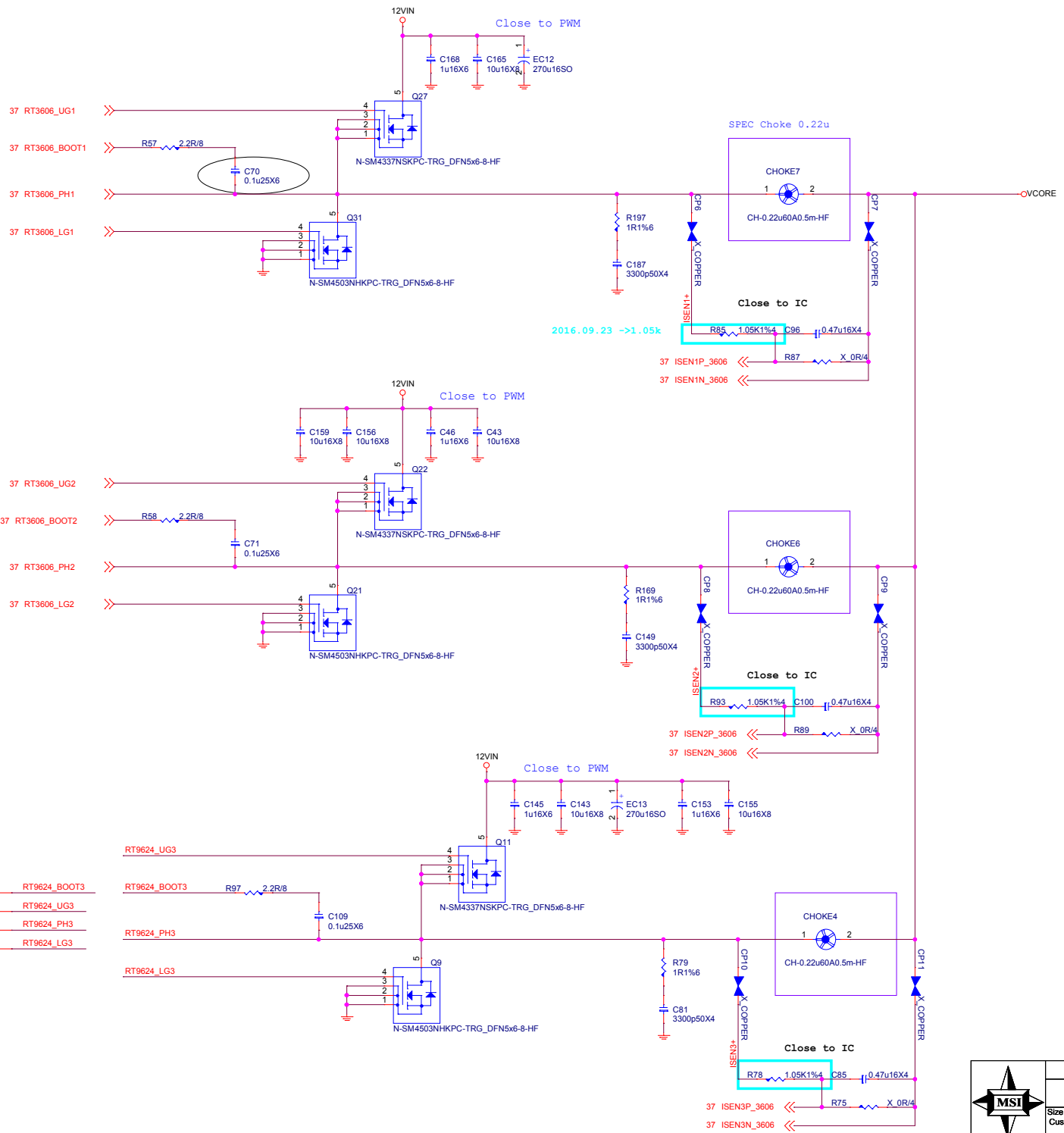
Size	Document Description	Rev
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20151106 Modify

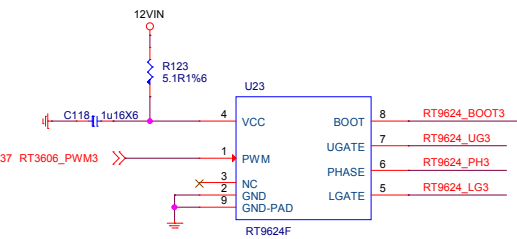
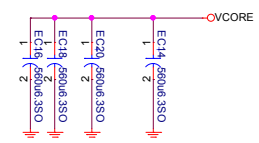


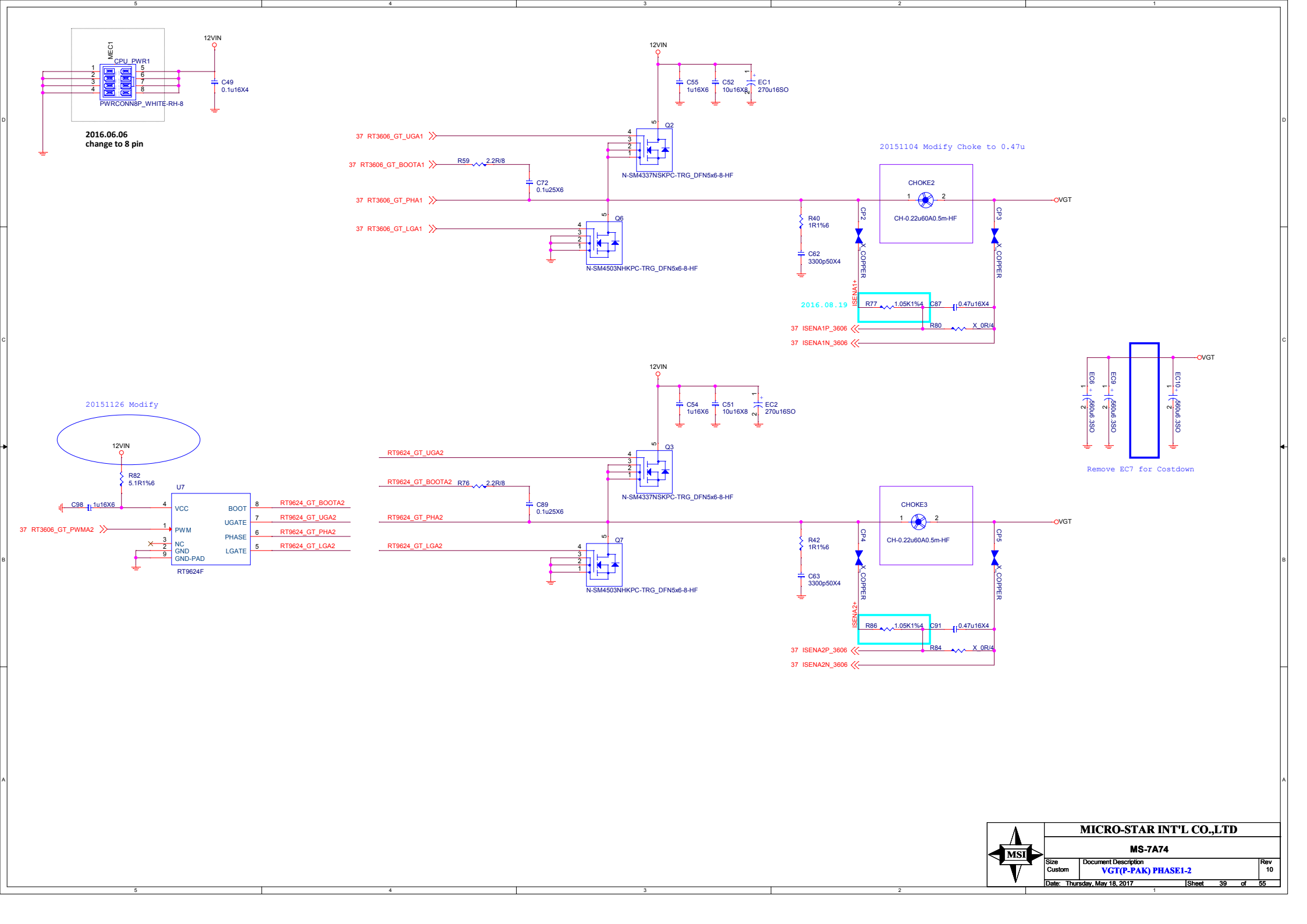
SLP_S3# assertion to IMVP VRM_EN deassertion
max:1us





ICCMAX: 78A
LL: 2.1m ohm





DDR4_1.2V 2.8A+ 4.75A+0.375A=7.925

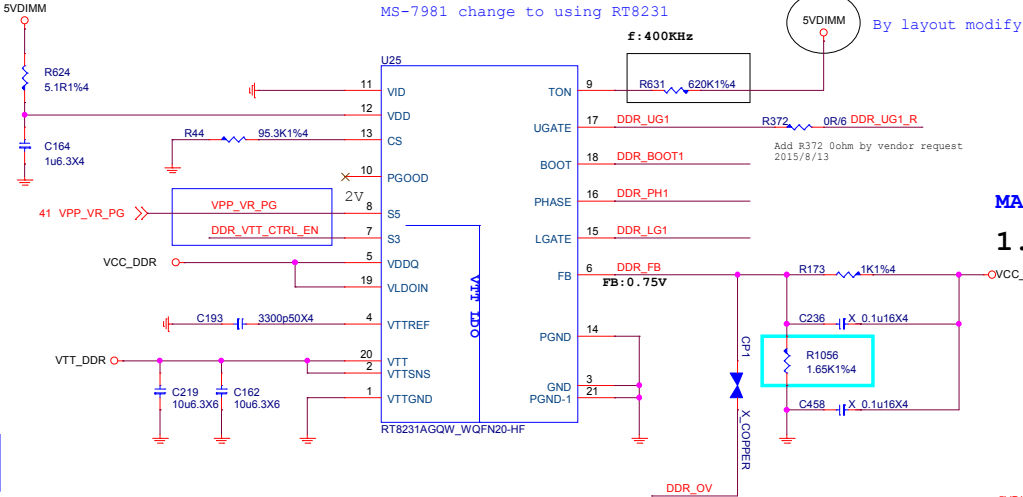
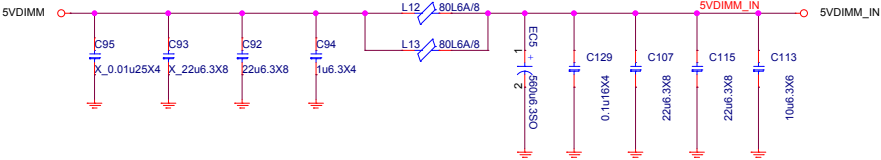
2.8A FOR CPU
4.8A FOR 2DIMM DDR3
0.375A FOR VTT_DDR

OCP = 7.925A * 1.5 = 11.8875A
Current limit = 95.3K(R1054) * 5uA / 10 / 4mohm = 11.91A

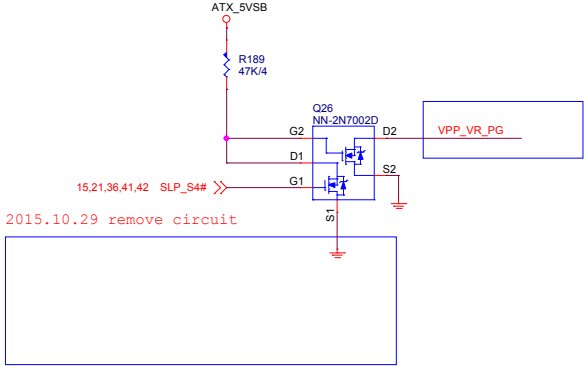
2015.04.23 change to RT8231

VID	Reference Voltage (V)
H	0.675
L	0.75

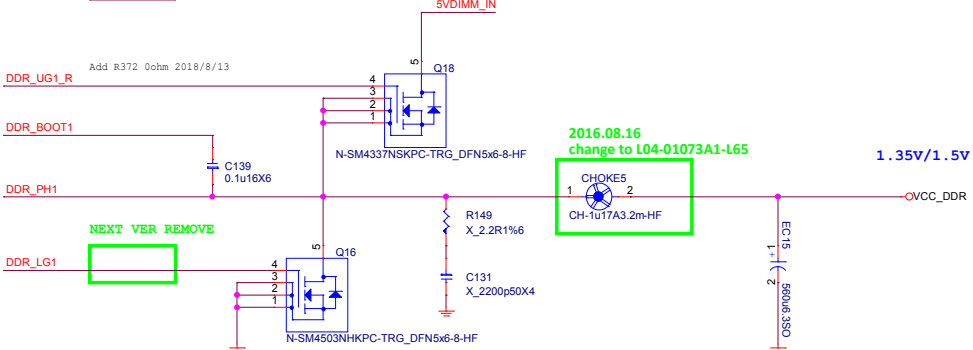
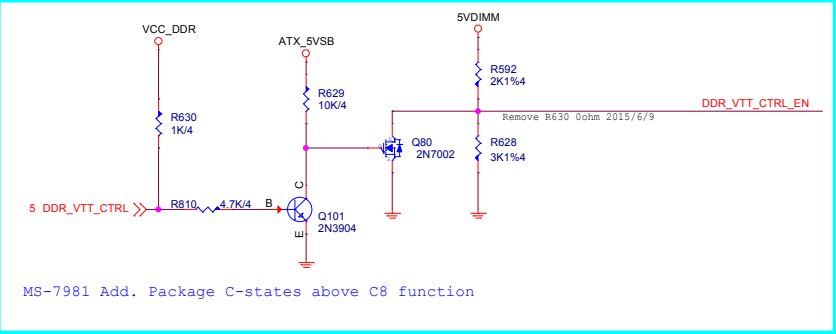
$I_{rms} = I_{out} * \sqrt{((V_{out}/V_{in}) * (1 - (V_{out}/V_{in})))}$
 $= 7.925 * 0.42$
 $= 3.384A$



MAX: 7.925A
1.2V



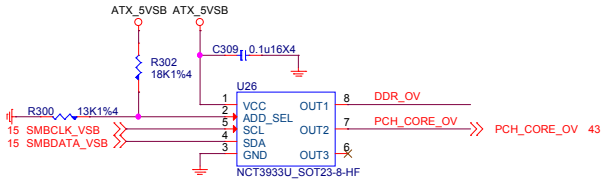
SLP_S4# de-assertion to VDDQ ramp down start
VPP ramp down after VDDQ ramp down



1.35V/1.5V

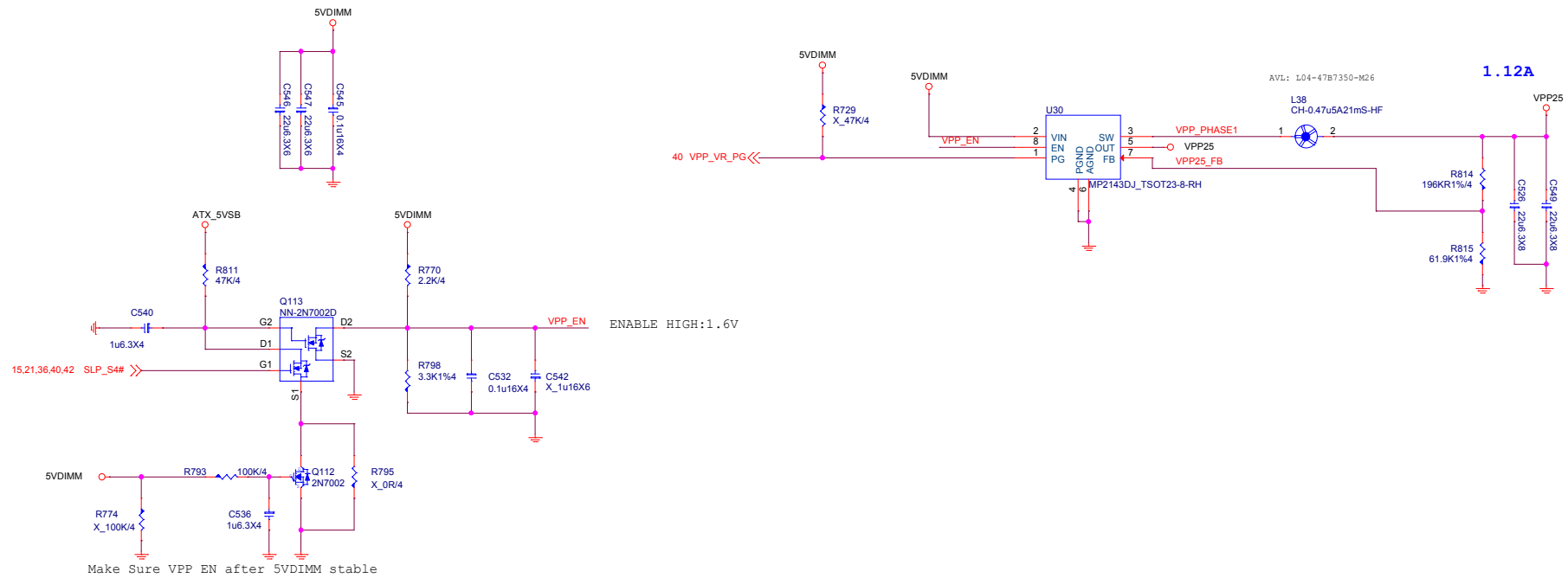
UPI VOLTAGE CONSOLE

0x26: RH=18K, RL=13K



2DIMM :1.12A FOR DDR VPP2.5V

VPP25 Power
2.5V; 1.12A



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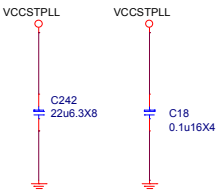
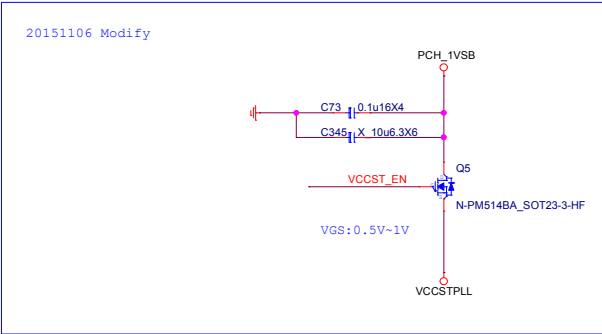
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VCCSTPLL

1.0V; VCCST: 60mA, VCCPLL: 150mA=60+150=210mA
For Cost down VCCST&VCCPLL merge

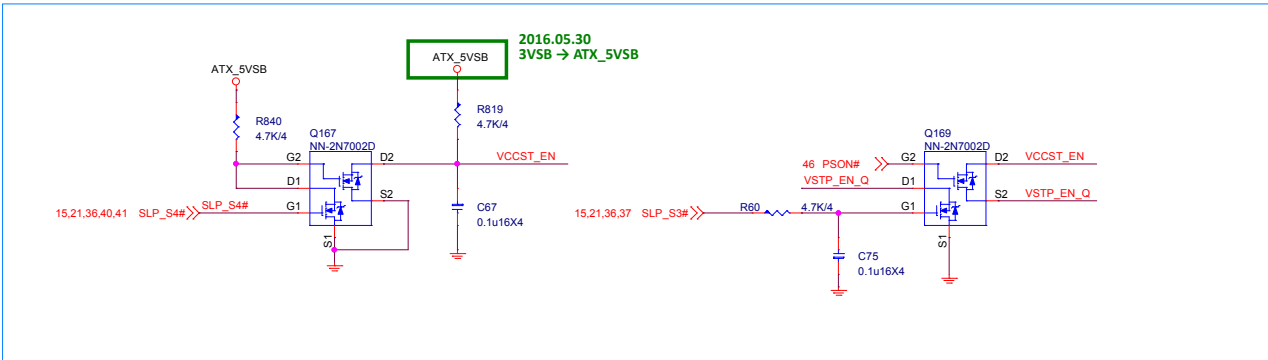
MAX: 210mA



Main:D03-514BA09-N03
AVL:D03-0341409-A68,D03-P500209-N03 ?

VCCIO ramped and stable before
beginning of VCCOPC/VCCEPIO ramp

VCCST/PLL stable 1ms before PROCPWRGD

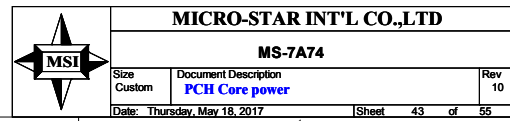


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$$1.0V; 8.572A+5.5A+0.21A=14.282$$
$$\begin{aligned} \text{Rocset} &= 1.5 * \text{Imax} * \text{Rdson(10)} / \text{Iocset} \\ &= 1.5 * 14.282 * 3.6\text{mohm} / 10\text{uA} \\ &= 7.71\text{K} \end{aligned}$$

```
Rocs:7.68K,OCP:
D03-4C05N03-O05 : 15.36A
D03-632BA0C-N03 : 16.69A
when use UBIO MOS Rocs:7.68K OPC:21.33A
```

D03-4C05N03-005 : 5 mohm
D03-632BA0C-N03 : 4.6 mohm
D03-3116M00-U47 : 3.6mohm



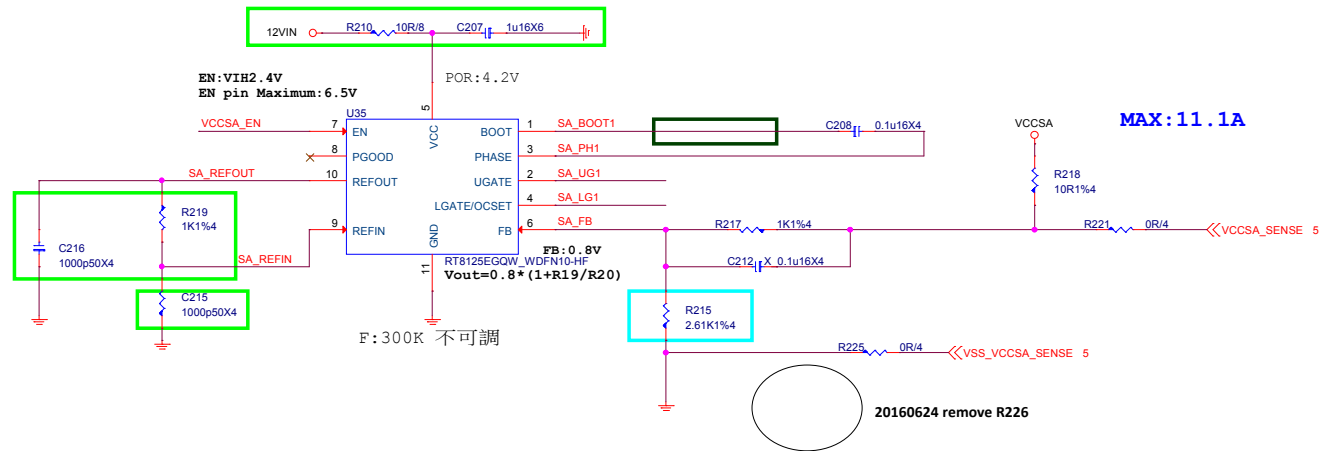
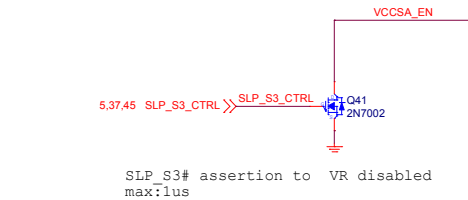
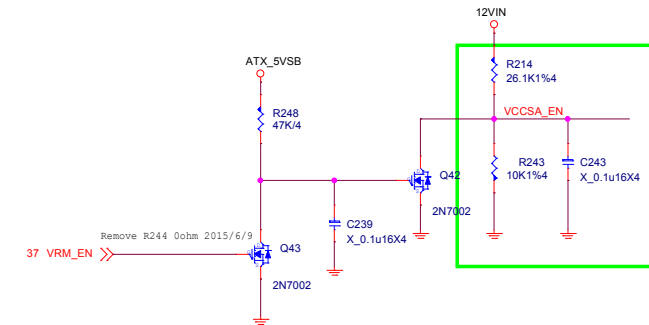
SA Power:1.05V,11.1A

$OCP = 11.1A * 1.84 = 20.44A$
 $R_{ocs}(R15) = OCP * R_{dson}(Low\ side) / 10uA$
 $= 20.44 * (2.5)mohm / 10uA$
 $= 5.11Kohm$

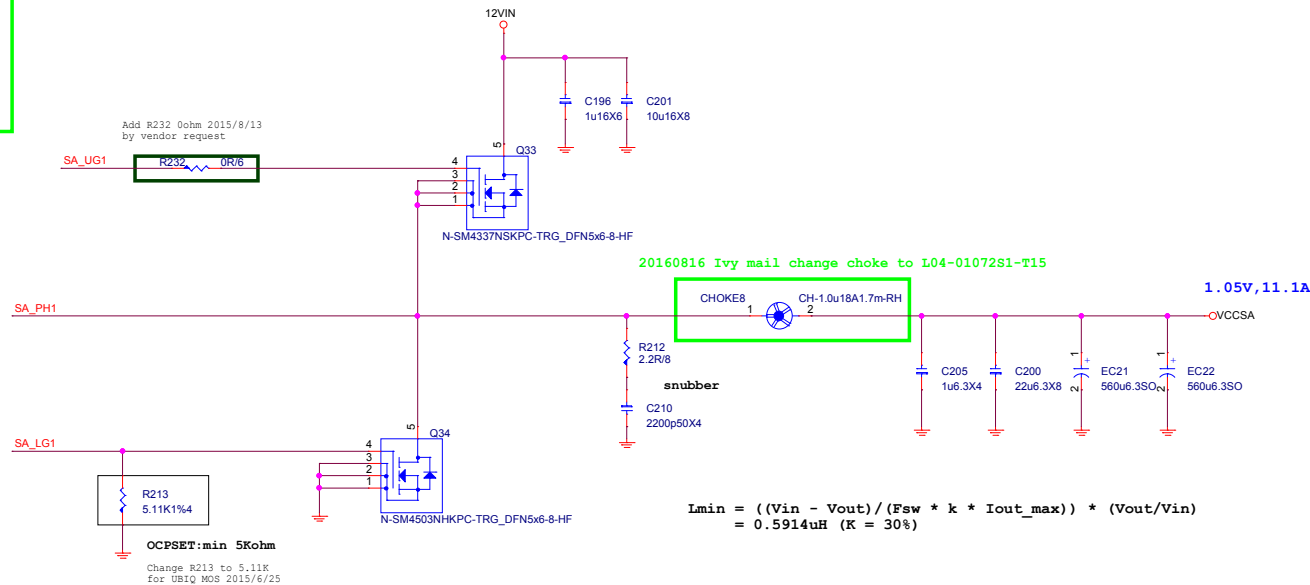
Rocs: 5.2836K, OCP:
D03-4C05N03-O05 : 15.76A
D03-632BA0C-N03 : 16.24A

Rocs: 5.11K
when use UBIQ MOS : 20.44A

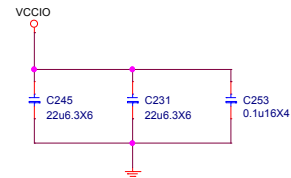
Rdson (low) 10V
D03-4C05N03-O05 : 3.4mohm
D03-632BA0C-N03 : 3.3mohm
D03-3056M00-U47 : 4.2mohm

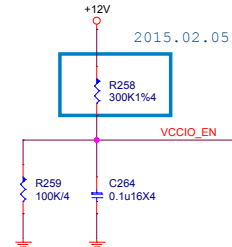
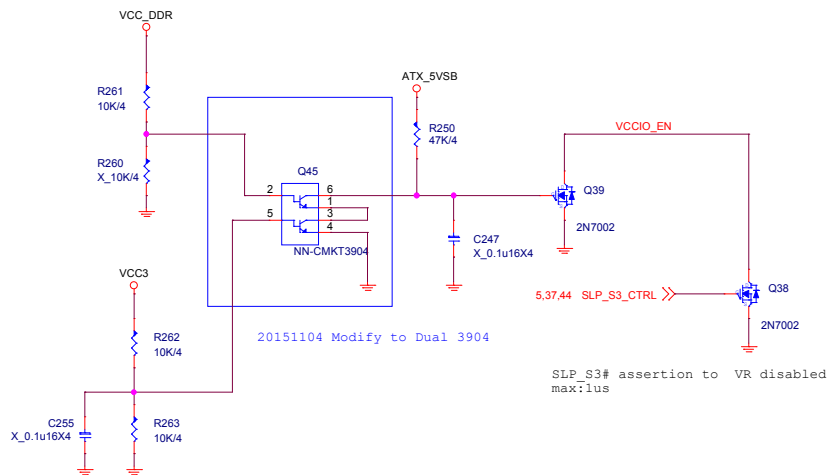


$$I_{rms} = I_{out} * \sqrt{(V_{out}/V_{in}) * (1 - (V_{out}/V_{in}))}$$
$$= 11.1 * 0.2825$$
$$= 3.13575A$$



0.95V; 5.5A

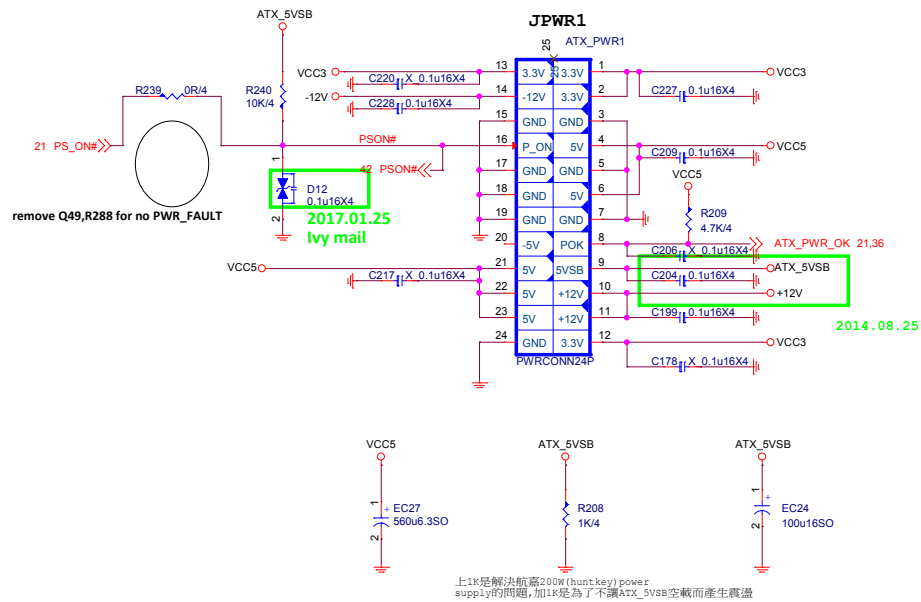

$$T_{ss} = (1/3) * ((V_{out} * C_{ss}) / I_{ss}), I_{ss} = 9\mu A$$

$$T_{ss} = (1/3) * ((1 * 22n) / 9\mu A) = 0.814mS$$


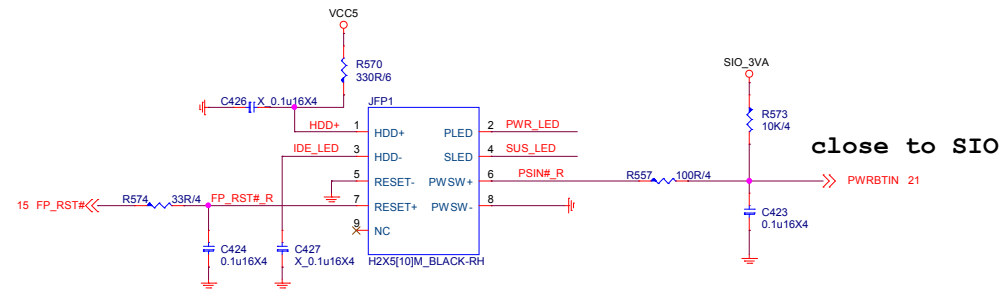
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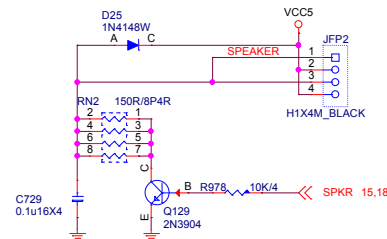
ATX POWER CONNECTOR



FRONT PANNEL



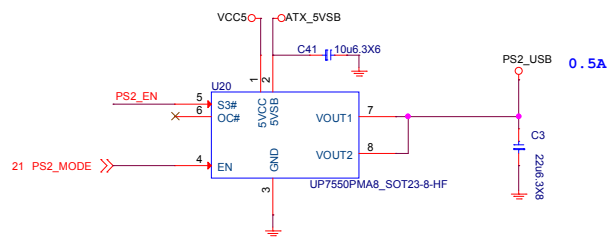
Speaker Pin Header



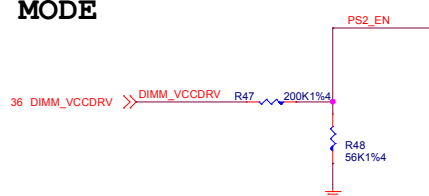
BEEP CIRCUIT

2016.06.02 Ivy mail
remove BEEP Circuit

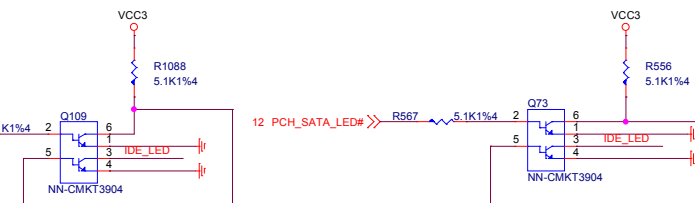
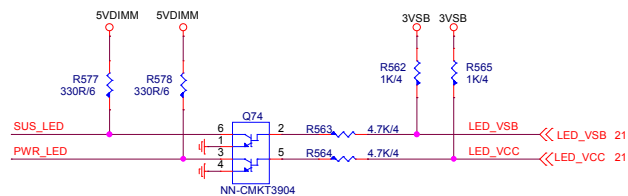
PS2 POWER



USB MODE



LED (for NV5533)



TPM

8/10 remove JTPM1

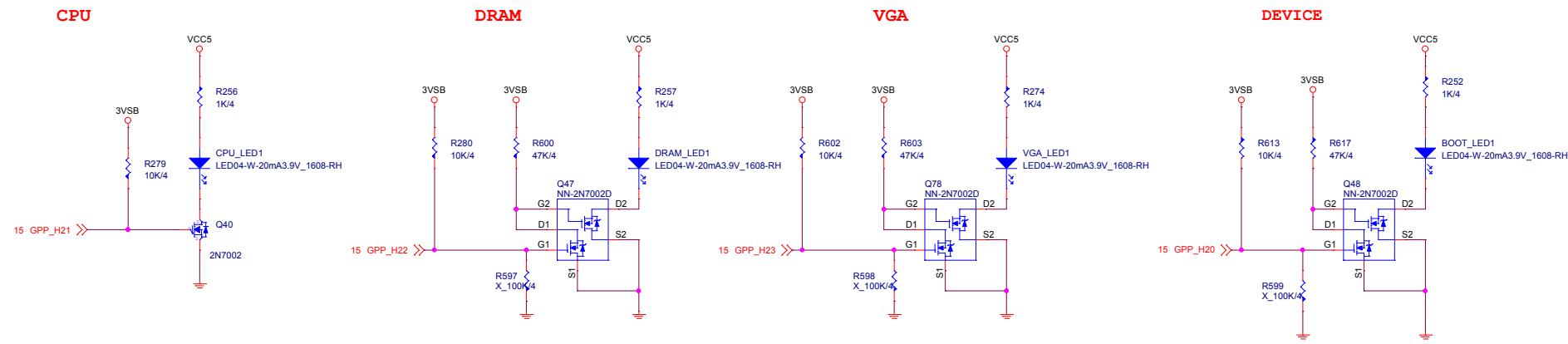


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DEBUG LED

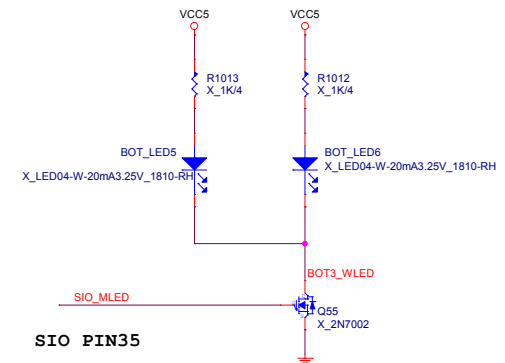
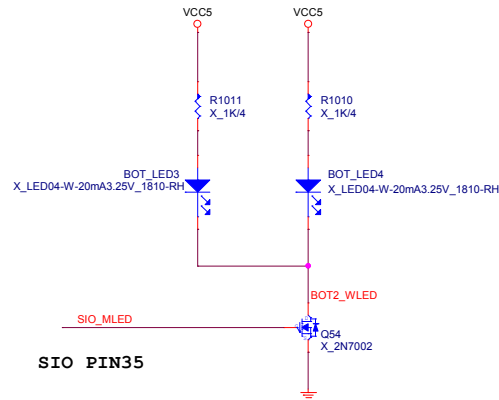
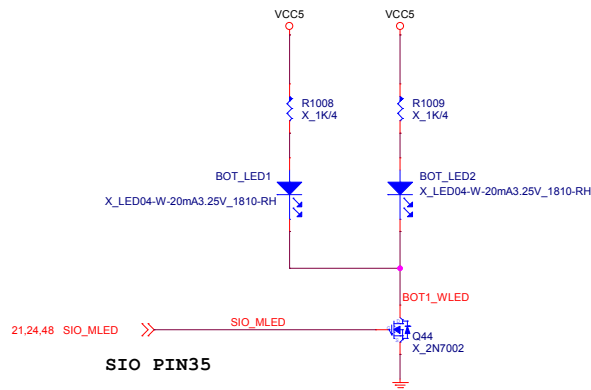


LED \	PCH_GP20	PCH_GP21	PCH_GP22	PCH_GP23
亮	NATIVE PULL HIGH	GPO PULL HIGH	GPO PULL HIGH	NATIVE PULL HIGH
滅	NATIVE LOW	GPO LOW (default LOW)	GPO LOW (default LOW)	GPO LOW (default LOW)

LED
RED:D0C-040P100-H91
AVL:D0C-040S500-E07

WHI:D0C-040T200-H91
AVL:D0C-040S200-E07

- 開機斷電狀態下，3個LED先維持default全暗，開機通電後：
1. 首先進行CPU checkCPU LED 亮，check PASS後則CPU LED滅掉。
 2. 接著依序進行Memory /memory LED亮check PASS後則memory LED滅掉。
 3. VGA的check/VGA LED亮，check PASS後則VGA LED滅掉。
 4. 因此最後正常順利開機後，三個LED燈都是滅掉的。（系統重啟或其他原因造成系統重開機，則LED仍按上述行為動作）



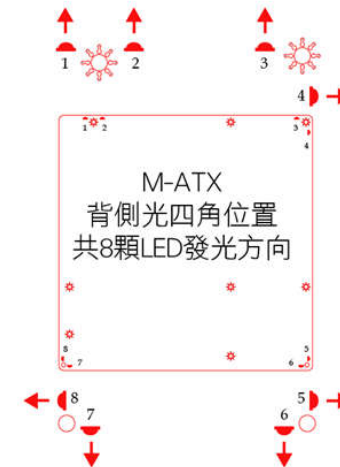
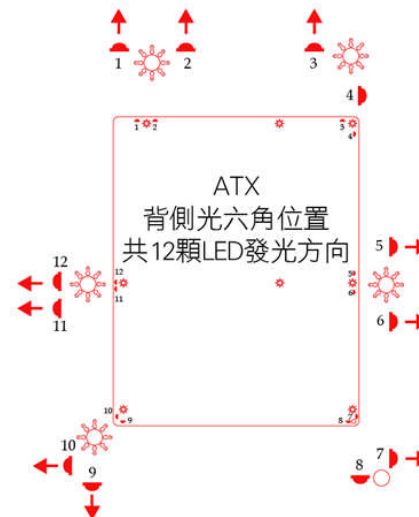
10/11 PM requires to remove ALL BOT LED

LED
紅 : DOC-040S600-E07


LED
白 : DOC-040T300-H91
AVL: DOC-040S300-E07



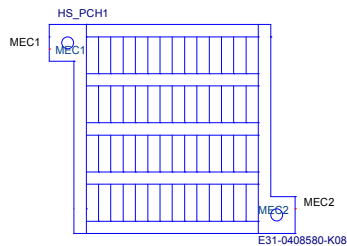
0824 remove BOT_LED7 & BOT_LED8



EMI CAP

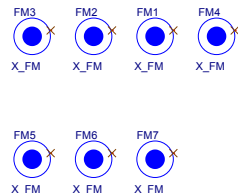


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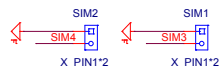


2016.09.23 HS change to E31-0408580-K08

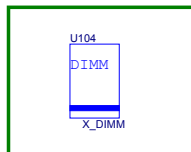
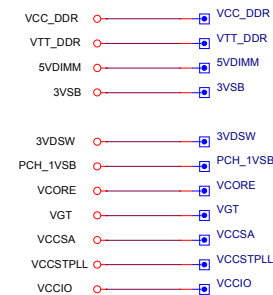
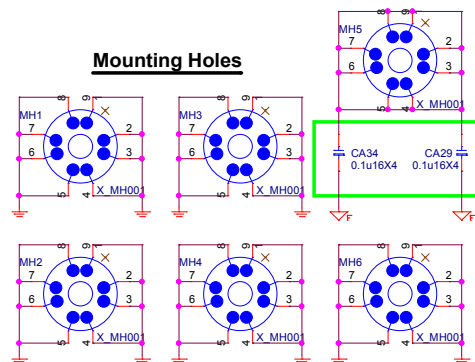
Optical Fiducial Marks-120



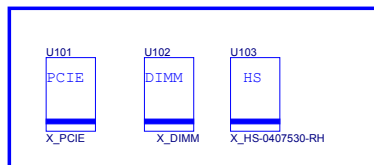
Simulation



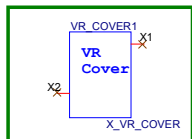
Mounting Holes



2016.11.18 change DIMM for Opt.E/F



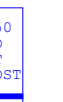
2016.10.26 change PCIE slot + DIMM + HS for B250M G1 GAMER



20160621 PM Request

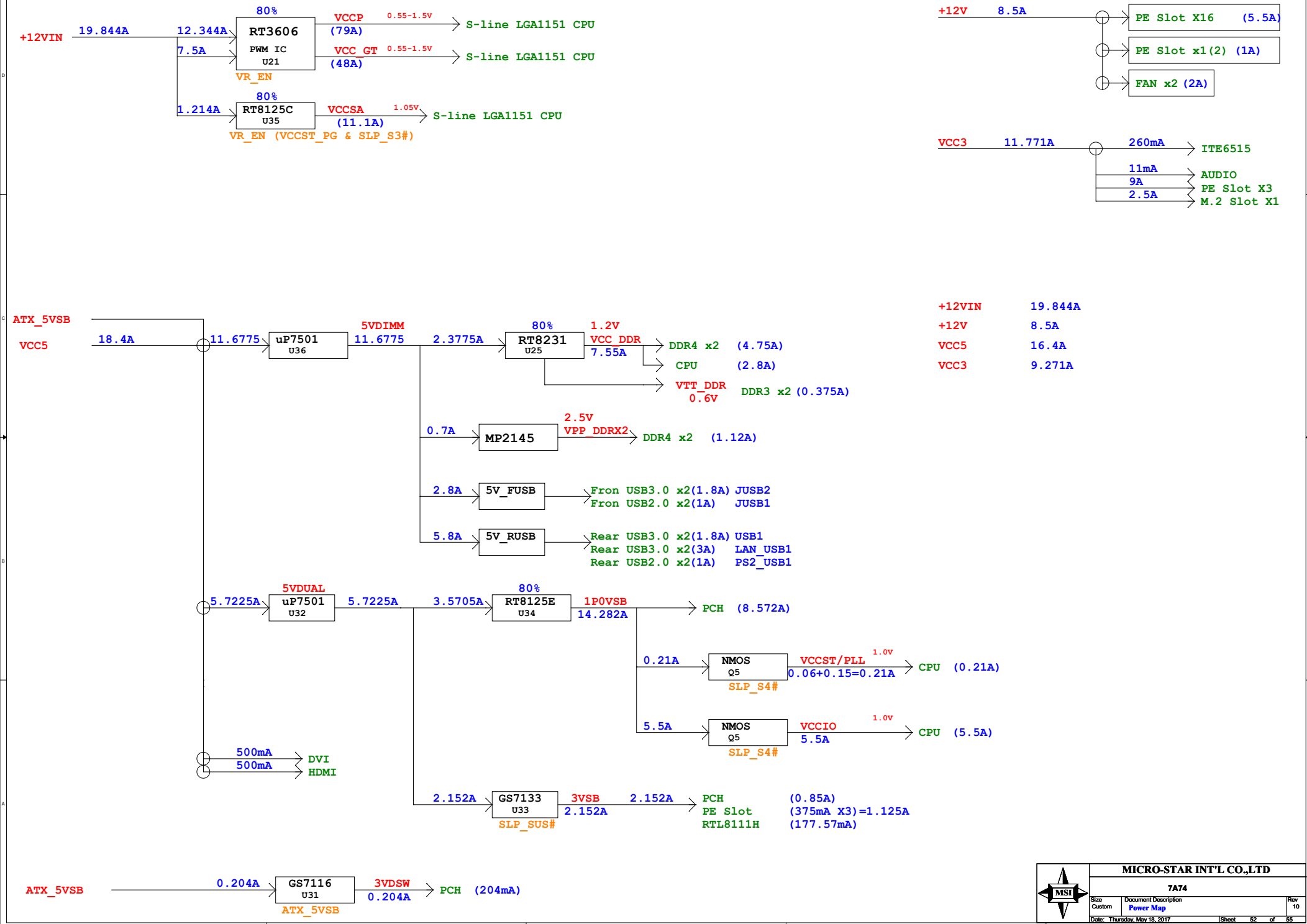


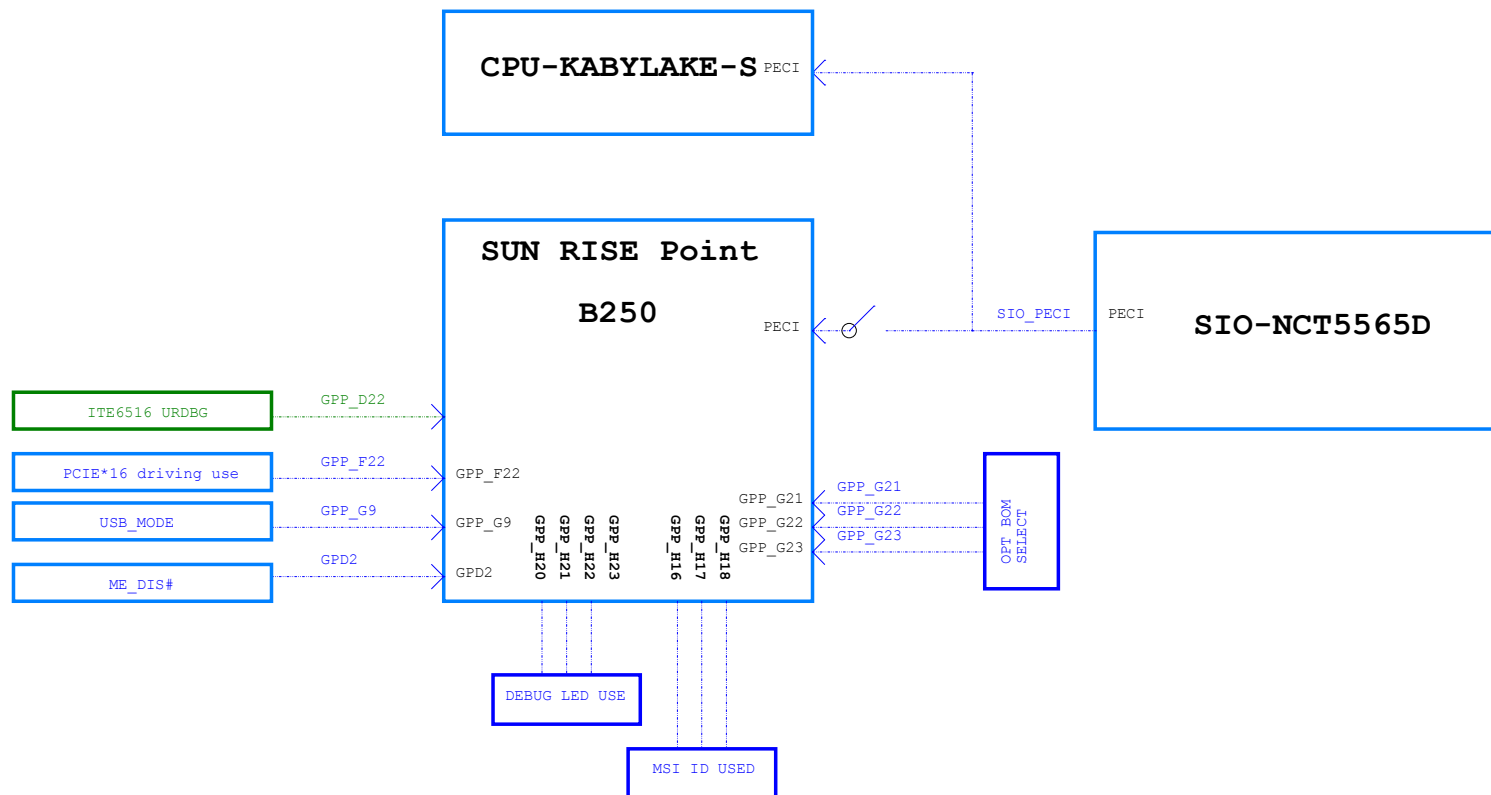
Marketing Name貼紙



PK0-07A7410-E48, 競華, 23, 寶安恩斯邁廠 (MSIS)

Power Delivery





(G3)DS5 ---> S0

VCCRTC (MB-->PCH)

RTCRST# (MB-->PCH)

ATX_5VSB (By PSU)

3VDSW (By ATX_5VSB)

SIO_DPWROK (SIO-->PCH)

SLP_SUS# (PCH-->SIO)

SYS3VSB_OFF (By BJT)

3VSB (By SIO)

5VDUAL (By SIO)

PCH_1VSB (By 3VSB)

RSMRST# (By SIO to PCH)

PWRBTN# (to SIO to PCH) (CP Internal 16ms debounce)

SLP_S5# (By PCH to ???)

SLP_S4# (By PCH to SIO)

SLP_S3# (By PCH to SIO)

PSON# (By SIO to PS)

VCCSTPLL (By SLP_S4#)

12V/5V/3V (By PSU to MB)

ATX_PWR_OK (By PSU to MB)

5VDIMM (By S3 & S4 & ATX_PWR_OK)

VPP25 (By S4 & 5VDIMM)

VCC_DDR (By VPP25)

VTT_DDR (By VCC_DDR)

VCCIO (By SLP_S3# & VCC_DDR)

IMVP8_EN (By SLP_S3 & VCCIO_PG)

VCCSA (By SLP_S3 & VCCIO)

VRM_PG (By VCCSA)

VCCST_PWRGD (By VRM_PG to CPU)

PCH_PWROK (By VRM_PG to PCH)

PCH_CLKOUT (By PCH_PWROK)

CHIP_PWGD (By SIO to PCH)

CPU_PWRGD (By PCH_PWROK (PCH to CPU)

PLTRST# (By PCH to SIO)

SVID (By VCCST) (Pull up with VCCSTPLL)

VCORE (By SVID)

VGT (By SVID)

DRAM_RESET# (By PCH_PWROK)

S0 --> S5

PLTRST# (By SIO to PCH)

CPU_PWRGD (By PCH to CPU)

PCH_CLKOUT (By PCH)

SLP_S3# (By PCH to SIO)

CHIP_PWGD (By SIO to PCH)

VRM_EN (By S3# Reverse)

VCCIO_EN

VRM_PG

VCCST_PWRGD

PCH_PWROK (By VRM_CORE_PG)

VCCIO

VCORE

VCCSA

PSON# (By SIO to PS)

ATX_PWR_OK (By PSU)

12V/5V/3V

SLP_S4# (By PCH to SIO)

DRAM_RESET# (By PCH to DIMM)

VCC_DDR

VPP25

THERMTRIP#

SVID

VCCSTPLL

SLP_S5# (By PCH to ???)

S5 --> D85

SLP_SUS# (By PCH to SIO)

SIO_SLPUS (by SIO to PCH)

3VSB (PCH_1VSB)

RSMRST# (by SIO to PCH)

D85 --> G3

ATX_5VSB

3VDSW

PCH_DPWROK (by SIO to PCH)



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